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Novel Techniques for Noise-Tolerance in Combinational Critical-Path Circuit Components

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Abstract: ***The continued scaling of the device and interconnect in the deep submicron jurisdiction of the complementary metal oxide semiconductor (CMOS) very large scale design (VLSI) has brought many new design challenges and exposed the limitations of the traditional VLSI design. One of the most severe problems in the deep submicron is that the circuit tend to malfunction by producing incorrect outputs in the event of inputs that have glitch. Such noise problem has emerged as the critical reliability problem in the deep submicron, in addition to the power dissipation problem. In this proposal, new research is proposed to counter the noise problem through novel circuit design techniques and methodologies. As we continue in deep submicron, the reliability of such designs is reduced as the output levels of such circuit suffer because of voltage scaling. We present our research along with the results and then describe the further proposed research. The research techniques are described using the combinatorial gates which serve as the critical path component in many designs. Also, an efficient flip-flop CD, that is conditionally discharged when there is no input changes and the input remains high to high, is proposed. This new flip-flop reduces the switching state activity, and is almost glitch-less at the output. The results from our proposed techniques demonstrate at least 2.3x the noise-immunity over the best known results in the literature.***

Keywords : Noise-immunity, Efficient flip-flop, VLSI design, CMOS

I. INTRODUCTION

Despite the recent research advances in designing noise-tolerant circuit, there is a vast gap between the noise-tolerance provided by such research and the noise-tolerance that will be actually needed in the very deep submicron (VDSM) in order for the designs to function correctly. For example, circuit components and design styles have been proposed that provide about 1.5 times to 2 times more noise immunity than the traditional VLSI design techniques. Although such level of noise-immunity may provide impressive results above the deep submicron level and also just at the edge of the deep submicron, they will almost certainly be insufficient to avoid functional failures in the VDSM. The continued voltage scaling and the increased operating frequency requires increased noise-tolerance for correct operation. Noise immune dynamic circuit was introduced in [1].

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The authors in [1] were the first pioneers in studying noise-immune circuits. In [2], the authors introduced crossbar architecture logic design with high reliability. Novel noise-immune dynamic gates were presented in [3]. Enhanced noise immunity techniques for dynamic logic was introduced in [4]. Designs of wide fan in dynamic logic for many gates were proposed in [5]. The authors in [6] Designed Dynamic Gates that are aware of Noise existence. In [7] and [8] they discussed design techniques for process voltage variations.

An Example of Bad Logic Problems in DSM

Existing design unit of logic gates such as XOR has a noise induced glitch problem [9]-[10]. The XOR design in Fig. 1 induces corrupted logic outputs. Such circuits need supply voltages that are at least 3.8 volts. They misbehave at low voltages. Reliable circuits are required at low voltage supply. They should provide correct output even in noisy non-immune environment. Test pattern for Crosstalk Induced Glitches are utilized and the output for gates {10]-[11] is depicted in Fig. 2.The circuit produces bad logic levels when input 'B' is low.

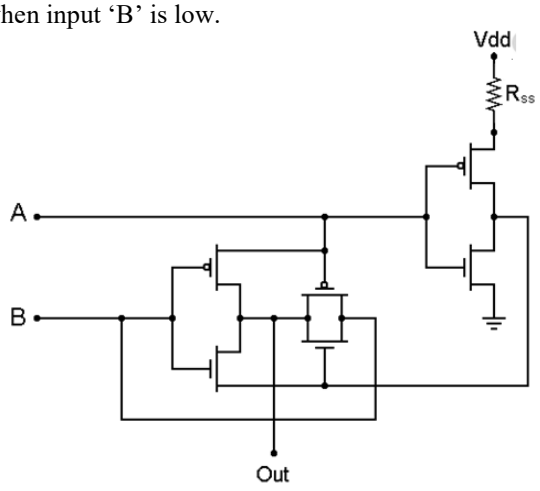

Fig. 1. Prior implementations for XOR function.

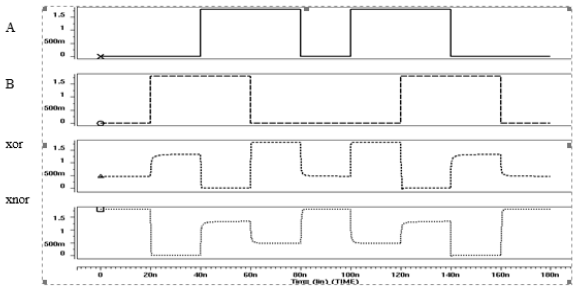

Fig. 2. Output of existing XOR gate at 1.8v at 0.18µ.

II. METHODOLOGY

2.1 Proposed Feedback-based Methodologies for Critical Path Components

A novel design for power-efficient noise-immune XOR- is proposed. Simulation using Hspice at voltage starting from 0.6V to 3.3V has been implemented. The results presents that the proposed circuit is more noise-tolerant and consumes less power. We added a feedback circuit between the XOR –gate and the ground. We utilized replicated transistors to specifically correct the output levels at specific inputs. This is shown in Fig. 3.

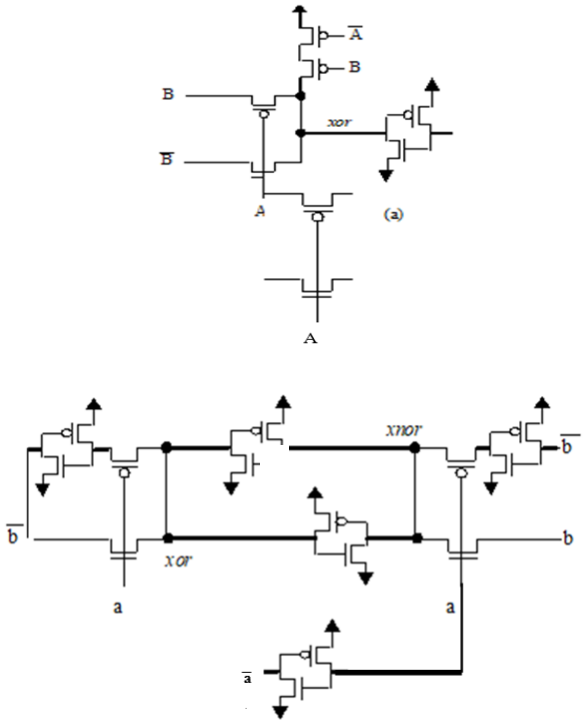

Fig. 3. Proposed XOR with noise tolerant circuit.

III.RESEARCH RESULTS

The Comparison of worse case delay and the noise curves are graphed in Fig. 4.(a) and (b). We plotted the Pulse Duration Tn in (ns), against the pulse amplitude PA in volt. This comparison of the proposed XOR with existing XOR design shows that noise immunity curves are higher which implies it can tolerate more noise (the area under the curve is larger). The area under the noise curve of the presented XOR is 2.41 times higher than the existing XOR.

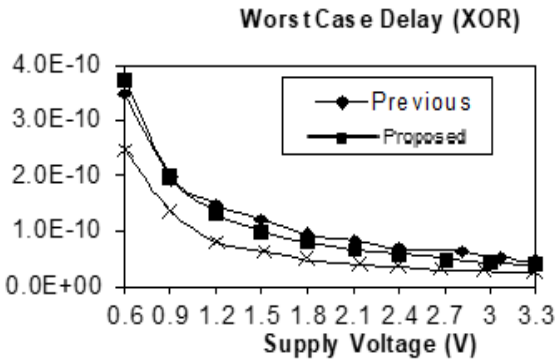

Fig. 4. (a) Comparison of worse case delay

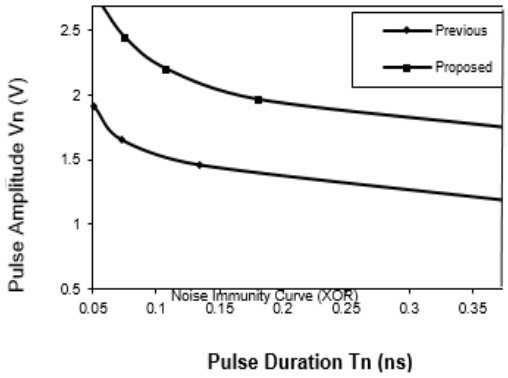

Fig. 4. (b) Comparison of noise tolerance

A novel design for noise-tolerant XOR- circuit is proposed. The novel XOR can operate at low voltage. Comparison between the proposed XOR and other XORs that can operate at low voltage is performed. The proposed circuit is almost glitch-less and noise tolerant. The noise immunity metric for the proposed circuit 1 is 2.16 times better than the existing XOR.

Proposed Research-Targets

We propose to investigate and address the following problems:

- Full development and generalization of the proposed single and double feedback based techniques for complex circuit for significant gain in noise-tolerance.
- Development of techniques that provide tradeoffs among noise-tolerance, power dissipation, and area for pass-transistor based designs.

IV.PROPOSED RESEARCH FOR NOISE-TOLERANT, HIGH PERFORMANCE, AND LOW POWER MEMORY ELEMENTS

We propose to investigate new techniques for design of flip-flops that are power efficient, noise tolerant, and high speed. The existing methods lack in several areas and there is an ever increasing need to come up with innovative designs to address the critical problems of power, speed, and noise. The preliminary results demonstrate the promise of the proposed technique.

Related Research

The clock system, its interconnection circuit and timing is power dominant and noise-critically intolerant circuits in a VLSI designs. It dissipates more than 50% of the total power in a system [2]. Methods for decreasing power dissipation of flip-flops, and increasing their noise-tolerance, is very crucial. The existing flip-flop design techniques are Conditional Precharge - based on the approach the flip-flops use to prevent redundant internal switching activity. Internal nodes are evaluated every clock cycle while the input is stable [4]. The Condition Captured Flip-Flop attempts to reduce redundant power at the internal node.

Proposed Conditional Discharge Technique and Proposed Flip-Flop

A central focus is to introduce a new design. An efficient flip-flop, which Discharge conditionally is proposed.

It utilizes a new technique that decreases, to a great extent, the switching activity, and eliminates output glitches. The proposed design reduces the flip-flop Energy-Delay-Product or EDP.

The flip-flop design implements the LOW-to-HIGH (LH) switching action such as if D is in HIGH state, the internal nodes are totally discharged. On the other hand, it implements the HIGH-to-LOW (HL) input state transition, such that If D is LOW then the LH action become disable. The proposed discharge technique is depicted in fig. 5. Also, The proposed CD flip flop is presented in Fig. 6.

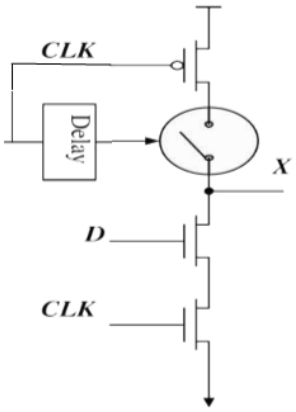

Fig. 5. Proposed Discharge Technique

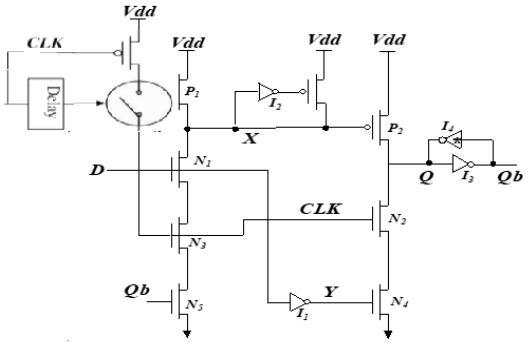

Fig. 6. Proposed CD flip flop

V. RESEARCH RESULTS

Simulations, using Hspice, are implemented for the existing and proposed flip-flops utilizing 1.8-V 0.18-mm CMOS. The simulation environment is shown in Fig. 7(a). The flip flop underwent an eight input data cycle with average power dissipation activity. The Clock frequency was set to 270 Mhz. Comparison utilized Energy-Delay and Energy-Delay-Product curves. Power consumption of the proposed flip flop is reduced by 22.5% at target D-to-Q delay of 67 ps, and reduced by 40% at 27 ps. Fig. 7(c) shows the EDP curve showing better performance of the proposed method. Fig. 8(a) and 8(b) depicts the comparison of the waveforms for the existing and proposed flip-flops. The output waveforms of the proposed flip-flop are glitch-free when the input is HIGH-HIGH (HH).

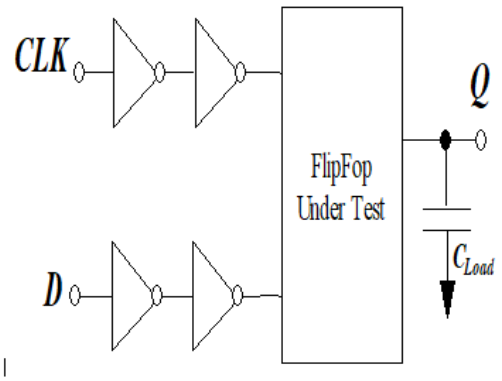

Fig. 7. (a) Simulation Setup

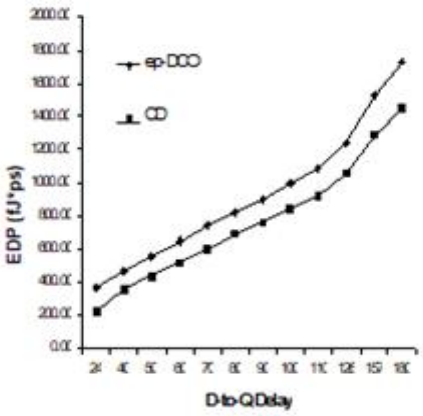

Fig. 7. (b) Delay-to- Energy curves

Table I. Comparison of the proposed flip flop with other existing flip-flops design.

	Number of transistors	Clocked transistors	Power dissipation (uW)	Energy (fJ)
CP-SAFF [14]	24	3	22.8	11.98
DE-CPFF[13]	33	21	23.6	4.87
CPFF[12]	23	12	22.3	4.34
Ep-DCO[15]	26	15	23.4	4.42
Proposed CD	28	15	19.2	3.54

The comparison of different flip-flops are depicted in table 1. We compared the proposed flip flop Cd with Flip-flops CPFF [12], DE-CPFF [13], CP-SAFF [14] and Ep-DCO [15]. The proposed CD has the least delay. Although, ep-DCO has a short delay also. The reason that ep-DCO has a short delay is that because it has short NMOS stack than pulsed D gates such as CCFF and CPF. The proposed CD has a strong driving capability that depicts shorter delay. A PDP comparison of CD and SAFF-CP implies that proposed gate has the smallest PDP because of the very small D-to-Q delay.

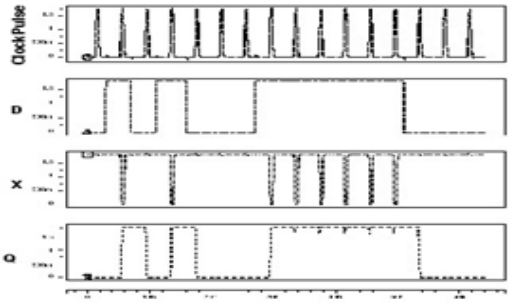

Fig. 8. (a) Glitches of the waveform of the ep-DCO

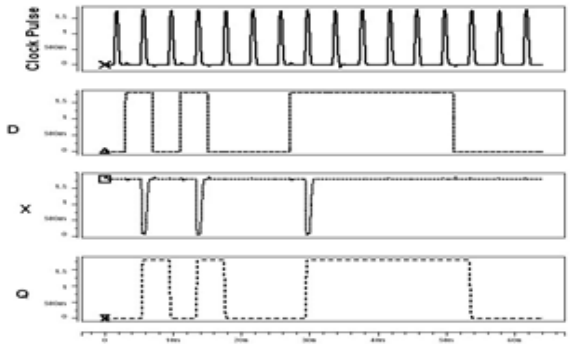

Fig. 8. (b) Glitch-less waveform of the proposed CD

We evaluated the noise robustness of the proposed CD flip-flop using noise injection circuit and noise immunity curves as described earlier. The noise immunity curves are depicted in Fig. 9. The proposed CD flip-flop is 1.754 times more noise-immune than the ep-DCO flip-flop (Table 2).

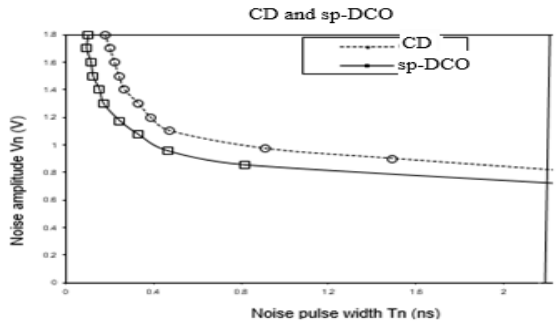

Fig. 9. Noise immunity curves for CD and sp-DCO

Table II. Noise immunity metric results for CD and ep-DCO

	CD	ep-DCO
Noise immunity metric	0.7324	0.4271
Improvement	1.73 X	

VI. CONCLUSION

A novel design for noise-tolerant XOR- circuit is proposed in this paper. The novel XOR can operate at low voltage. Comparison between the proposed XOR and other XORs that can operate at low voltage is performed. The proposed circuit is almost glitch-less and noise tolerant. The noise immunity metric for the proposed circuit 1 is 2.16 times better than the existing XOR. We proposed to investigate and address several problems. Full development and generalization of the proposed single and double feedback based techniques for complex circuit for significant gain in noise-tolerance. Development of techniques that provide tradeoffs among noise-tolerance, power dissipation, and area for pass-transistor based designs. Also, a novel technique of conditional Discharge is presented. New design of flip-flops with noise tolerant characteristics is presented. Switching of input states of 37.5% was employed for testing. The proposed flip-flop depicted saving of 39.6% of the consumed energy along with high speed.

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