International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-9 Issue-2, December 2019

Fuzzy Based Combined Feed-Forward and Feed-Back Controlled Dynamic Voltage Restorer for Enhanced Fault Ride through Capability in DFIG based Wind Turbines

Siddu Balarami Reddy, M. Ramasekhara Reddy

Abstract – In this paper, Fault ride through (FRT) capability is enhanced using dynamic voltage restorer (DVR) in a wind turbine-driven doubly fed induction generator (DFIG). For effective control of the DVR, Fuzzy based combined feed-forward and feed-back (CFFFB) voltage control is used. The performance of DVR using CFFFB with FLC control is observed during balanced and unbalanced conditions in terms of voltage sag mitigation, reduced THD, fault current control and dc-link voltage balancing. The advantage of control strategy is validated utilizing simulation of 1.5MW DFIG-WT and results shows better reactive power support during faults condition.

Keywords*: Doubly-fed induction generator (DFIG), dynamic voltage restorer (DVR), Fault ride through (FRT), combined feed-forward and feed-back control.

I. INTRODUCTION

In modern days, the impact of wind energy improvement is increased worldwide. Due to this positive force in improvement of wind energy is commonly amazing message for environmental transformation and clean imperative originators. In any case, the operators of the grid were not predicted this much growth in the wind energy so we require the grid code to sustain as stable operation in network. Fault ride through (FRT) is the most difficult grid code for wind farms and gives wide challenges for variable speed wind turbines under transient conditions. During fault conditions, wind farms never again allowed to separate from the grid, rather are required to supplying reactive power to grid and run as common power plants [1].

Among wind turbines (WT), DFIG are most supreme type due to their ability of variable-speed wind turbine and controllable of real power and reactive power. Despite fact that DFIG-WT are most popular type but the operation of the DFIG is susceptible to disturbances of grid. At fault instant, the DFIG voltage is reduces this leads to reduction in the generation of real power so for stabilize real power RSC increase rotor current.

Revised Manuscript Received on December 30, 2019.
***** Correspondence Author
Siddu Balarami Reddy*, M.Tech (student), Dept. of Electrical Engineering, JNTUA, Ananthapuramu, Andhra Pradesh, India.
M. Ramasekhara Reddy, Assistant professor, Dept. of Electrical Engineering, JNTUA University, Ananthapuramu, Andhra Pradesh, India.

© The Authors. Published by Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP). This is an open access article under the CC-BY-NC-ND license http://creativecommons.org/licenses/by-nc-nd/4.0/

Consequently, the RSC rises the voltage of rotor this leads to over voltages are occurred in dc-link. Generally, the crowbars are used to reduce the higher currents in the rotor to protect the converters during faults condition. But after the activation of crowbar system, the crowbar disconnects RSC and short circuiting the rotor through parallel resistance. Because of this existence of parallel resistors, DFIG consumes reactive power from grid and acts like induction generator rather of reactive power supporting to grid [2]. To reduce higher currents in rotor, additional approaches are recommended by crowbar with integration of dc-link chopper, series breaking resistor and static synchronous compensator (STATCOM) [3].

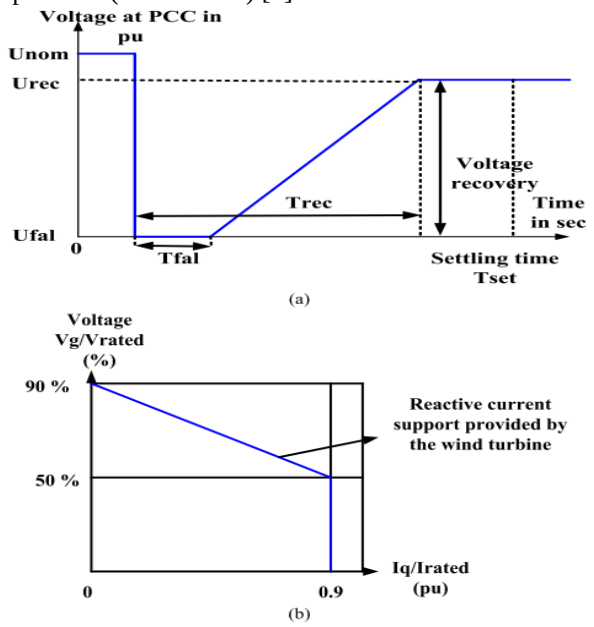


Fig.1. (a) FRT grid code. (b) grid code reactive power requirement

To enhanced FRT capacity, a couple of advanced methods are so far being suggested in DFIG-WT. For FRT capability the Germany setup the grid code requirements are appeared in Fig.1(a) and 1(b). even under faults the turbine must stay allied below the represented line which is displayed in Fig 1(a) and clearance of the fault must be 20% of rated power/sec. Reactive current abutment is to be obtained by wind turbines as delineated in fig 1(b) and these are to be completed within 20ms after fault instant [4].

STATCOM is a shunt device connected at PCC and used to give elevated performance in transient voltage control. Under fault conditions, the higher currents flow in rotor. To secure rotor side converter (RSC) from these higher currents the STATCOM takes the crowbar help. The STATCOM minimize the fault clear time and increased decelerating torque of generator. This result increases the stability region of the generator and mechanical pressure also increased. DVR implementation is a better explication and no need of protective circuit when operated. Fig 2 shows that generalized representation of DFIG with DVR. In contrast DVR is direct explication and more effective for voltage restoration at its load terminals when voltage is interrupted at source terminals [5].

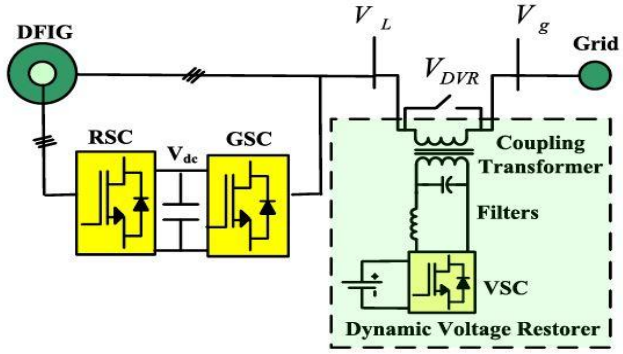


Fig. 2 .Generalized representation of DVR with DFIG

The effectiveness of explication of control technique implemented in DVR to enhanced FRT capability in DFIG is determined for various fault in grid. DVR control is obtained by various steps, that are reference generation, current and voltage modulation [6]. In Feed-Forward control, switching pulses for VSI is obtained by modulator by applying the reference voltage directly. Though it has advantages of simplicity, disadvantages like inferior transient response, and because of phase shift steady state error is occurred and voltage drop on series filter and injection transformer are present [7]. A feedback or combined feedback and feed forward controller are implemented to reduce above problems. In this circuit, measured voltage is returned to voltage controller. But this also has a poor THD values during transient period which produce high spike in power and voltage.

In this paper, DVR with fuzzy controlled CFFFB is used for voltage control. Enhancement FRT capability and THD in DFIG-WT using DVR with Fuzzy controlled CFFFB is discussed for both balance and unbalanced faults. Construction of the paper is as fallows. Section two confers about DFIG with DVR modelling, section three analyzes about DVR control and simulation results are tested under transient conditions and also hormonic mitigation is discussed in section four, followed by a conclusion.

II. MODELING OF DFIG AND DVR

Understanding of DFIG performance in transient conditions is important in order to implement advanced methods to enhanced the FRT capacity. In DFIG, stator is connected to grid directly and rotor is linked with slip rings and back-to- back voltage source converter (VSC) to grid. Here RSC and GSC are converters connected at rotor side and grid side respectively and both provides up to 25-30% of machine's total capacity.

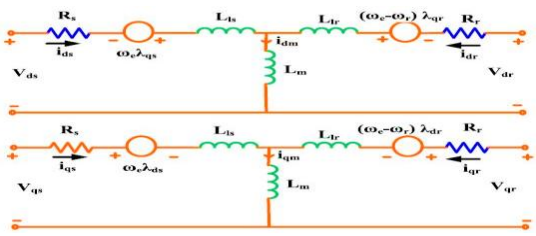


Fig. 3: DFIG equivalent circuit

DFIG equivalent circuit is simulate in synchronous dq reference frame shows in Fig.3. voltage, current and flux mathematical expressions shown below.

$$\begin{aligned} v_{ds} &= R_s i_{ds} + \frac{d\lambda_{ds}}{dt} - \omega_e \lambda_{qs} \\ v_{qs} &= R_s i_{qs} + \frac{d\lambda_{qs}}{dt} + \omega_e \lambda_{ds} \\ v_{dr} &= R_r i_{dr} + \frac{d\lambda_{dr}}{dt} - (\omega_e - \omega_r)\lambda_{qr} \\ v_{qr} &= R_r i_{qr} + \frac{d\lambda_{qr}}{dt} + (\omega_e - \omega_r)\lambda_{dr} \end{aligned} \quad (1)$$

Here v_{dqr} and v_{dqs} are voltage of dq rotor and stator. i_{dqr} and i_{dqs} are currents of dq rotor and stator. ω_e and ω_r are angular frequency of supply and rotor. λ_{dqr}, λ_{dqs} are flux linkages of dq rotor and stator respectively. R_r is rotor resistance, R_s is stator resistance.

$$\begin{aligned} L_s &= L_{ls} + L_m \\ L_r &= L_{lr} + L_m \end{aligned} \quad (2)$$

Here, L_r and L_{lr} are inductance and leakage inductance of rotor. L_s and L_{ls} are inductance and leakage inductance of stator. magnetizing inductance is Lm.

$$\begin{aligned} \lambda_{ds} &= L_s i_{ds} + L_m i_{dr} \\ \lambda_{qs} &= L_s i_{qs} + L_m i_{qr} \\ \lambda_{dr} &= L_m i_{ds} + L_r i_{dr} \\ \lambda_{qr} &= L_m i_{qs} + L_r i_{qr} \end{aligned} \quad (3)$$

Under stator flux-oriented control, reactive power (Q_s) is control by rotor d-axis current components and real power (P_s) is control by current components of q-axis rotor.

$$\begin{aligned} P_s &= \frac{3}{2}(v_{qs} i_{qs} + v_{ds} i_{ds}) \\ Q_s &= \frac{3}{2}(v_{qs} i_{ds} - v_{ds} i_{qs}) \end{aligned} \quad (4)$$

A.MODELING OF DVR

DVR is a VSC equipped with LC type filter and a coupling transformer and connected at PCC in series to DFIG-WT and grid to correct fault voltages in system. PWM technique is utilized to provide switching pulses to VSC. For synchronization, PLL is used to find phase angle. During faults, DVR inject the voltage into the system to maintain constant terminal voltage of DFIG-WT. as per grid code, DVR must provide the full voltage compensation under faults. Rating of DVR power in-phase compensation is shown below

$$S_{DVR} = \sum_{k=a,b,c} V_{DVR,k}^{ref} * I_L \quad (5)$$

$V_{DVR,k}^{ref}$ denotes the RMS value of DVR injection voltage in phase K. I_L denotes load current in RMS.

Change in real power between grid and DVR is shown below

$$P_{DVR} = P_L - P_g \quad (6)$$
$$= (3 * V_L * I_L * \cos) - \sum_{k=a,b,c} [V_{DVR,k}^{ref} * I_L * \cos \Psi]$$
$$V_{DVR,k}^{ref} = \sqrt{2} * \left| V_L - V_{g,k}^{ref} \right| \quad \text{and } k = a, b, c \quad (7)$$

DVR inject voltage with same phase angle of grid voltage.

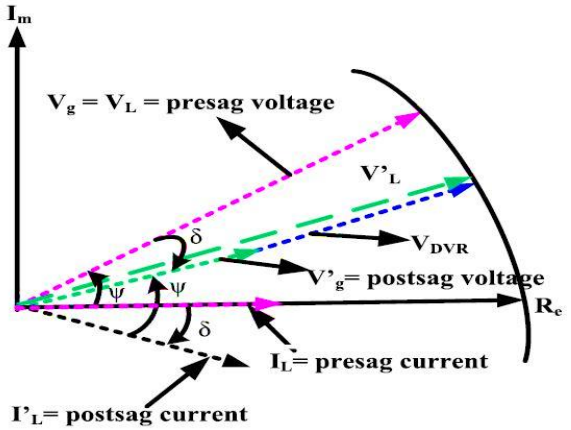


Fig. 4.Compensation scheme of DVR based on in-phase compensation.

Here, Ψ denotes phase difference between V_g and I_L before and after sag. δ represents phase difference between V_g' and V_g and also difference between I_L' and I_L shown in Fig 4.

III. DVR CONTROL TECHNIQUES

A.CFFFB CONTROL TECHNIQUE

Control technique of DVR should include reference generation, transient control, fault occurrence at start and end and also protection. On grid side, Pre-sag voltages are carried by Feed-Forward control to detect voltage fault before DVR. $V_{Ldref} = V_0$ (where V_0 represents ($V_{La}^*, V_{Lb}^*, V_{Lc}^*$)), is reference regulated by voltage of load bus respectively.

$$V_{La}^* = V_0 \sin \omega t$$
$$V_{Lb}^* = V_0 \sin(\omega t - \frac{2\pi}{3})$$
$$V_{Lc}^* = V_0 \sin(\omega t + \frac{2\pi}{3}) \quad (8)$$

Feed-Back control observes mitigation of voltage after DVR on DFIG side for protection of converter Dc-link voltage control is over seen. Both feed-back and feed-forward controls are included in combined control. During faults condition, immediate detection of voltage sag plays an important role for controlling. Balanced and unbalanced sag is calculated by phase jump. References of sinusoidal voltage are obtained by PLL using reference of load voltage and implemented for dq co-ordinate controller. Transient response is observed by Feed-Forward control on Dc-link voltage to obtain sag depth. To reduce steady state error Feed-back voltage control is performed. Implementation of FLC also helps in reducing the harmonics in the system during the fault periods. The control structure of FLC based CFFFB of DVR is shown in fig 5.

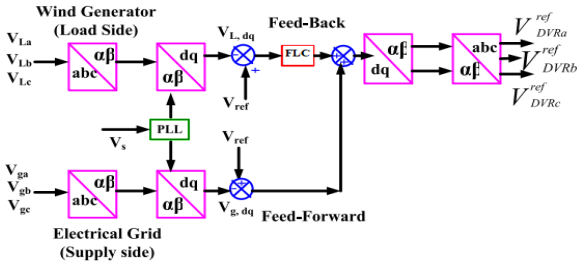


Fig. 5 Control Structure FLC-CFFFB of DVR.

B.FUZZY LOGIC DESIGN

Professor L.A Zadeh of university of California at Berkey initially designed the possibility of fuzzy logic in 1965. But it was not perceived before Dr E.H. Mamdani, utilized fuzzy controller in an application to controlled a programed steam motor in 1974. Increasing number of fuzzy usages accounted since 1980s incorporating in modern technology. In FLC numeric factor are changed into phonetic factors and controlled by arrangement of sematic rules.

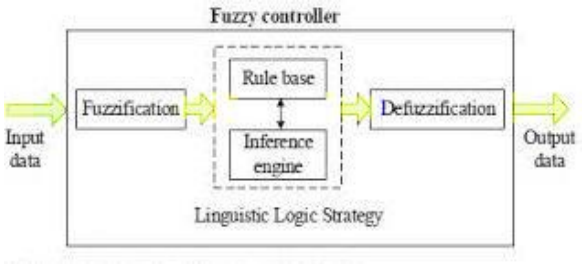


Fig. 6. Fuzzy logic controller

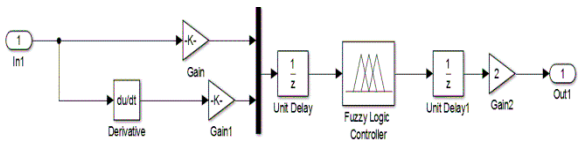


Fig. 7. Design of FLC

The FLC includes three sections: Fuzzification, inference and Defuzzification. FC is portrayed as i. seven fuzzy sets for each information and permit, ii. Triangular participation capacities for straight forwardness, iii. Fuzzification use persistent universe of talk, iv. Suggestion use Mamdani's, 'min' operator, v. Defuzzification utilizing stature strategy. Schematic diagram and structural diagram of the FLC is displayed in fig. 6 and fig. 7 respectively and in Table 1 shows the FLC rules.

TABLE 1: FLC rules

CHANGE IN ERROR	ERROR						
	NB	NM	NS	Z	PS	PM	PB
NB	PB	PB	PB	PM	PM	PS	Z
NM	PB	PB	PM	PM	PS	Z	Z
NS	PB	PM	PS	PS	Z	NM	NB
Z	PB	PM	PS	Z	NS	NM	NB
PS	PM	PS	Z	NS	NM	NB	NB
PM	PS	Z	NS	NM	NM	NB	NB
PB	Z	NS	NM	NM	NB	NB	NB

In FLC, the information scaling factor is planned such that the information esteems are -1 and +1. Triangular state of enrollment position indicates for a specific E(k). it has a single overwhelming fuzzy subset. FLC error is defined as

$$E(K) = \frac{Pph(k) - Pph(k-1)}{Vph(k) - Vph(k-1)} \quad (9)$$

$$CE(K) = E(K) - E(K-1) \quad (10)$$

TABLE 2. DFIG and DVR of Simulation parameters

Symbol	Quantity	Values and units
P_{DFIG}	Rated power of DFIG	1.5 MW
	Cut-in speed, cut-out speed	3 m/s, 20 m/s
w_s	Rated wind speed	11 m/s
V_s, f	Stator voltage/frequency	575 V/ 50 Hz
R_s	Stator resistance	0.023 pu
R_r	Rotor resistance	0.016 pu
L_{ls}	Stator leakage inductance	0.18 pu
L_{lr}	Rotor leakage inductance	0.16 pu
H	Generator inertia constant	0.685
V_{dc}	Nominal DC bus voltage	1150 V
	Converter rating	30 %
P_{DVR}	DVR capacity	1.5 MVA
L_{DVR}	DVR Filter inductance	0.1 mH
C_{DVR}	DVR Filter capacitance	1 μF
f_{DVR}	DVR Switching frequency	10 kHz
	DC-link voltage	300 V
	Series transformer ratio	1:1

IV. SUMULATION RESULTS AND DISCUSSION

The enhancement of FRT capability is analyzed with the help of FLC based CFFFB of DVR Using simulation for a 1.5MW of DFIG-WT connected to grid in MATLAB under balanced and unbalanced sag conditions. DVR rating is 1.5MVA and it is connected at PCC through series transformer with 1:1 ratio. The simulation results tested FRT capability of DFIG-WT for various faults. DFIG-WT simulation parameters shown in Table 2. The performance of FRT capability using DVR is examine during balanced sag and unbalanced sag for 5 cycles of duration from 0.7s to 0.8s and also analyzed mitigation of harmonics and faults under short circuit condition. Enhancement of FRT capability using DVR with the help FLC-CFFFB is explained below.

Case 1: 35% Balanced sag.
Case 2: 35% Unbalanced sag.
Case 3: short circuit fault.
Case 4: Harmonic spectrum analysis.

A. CASE 1: 35% BALANCED SAG

Operation of DFIG-WT using DVR is analyzed during 35% balanced sag of supply voltage. Operation of DVR during balanced sag is tested for 100ms between 0.7s to 0.8s and responses are shown in fig 8 and 9 under fault condition. The Fig 8(a) is supply voltage compensated by using DVR control shows in Fig 8(b). Fig 8(c) shows injected voltage of DVR.

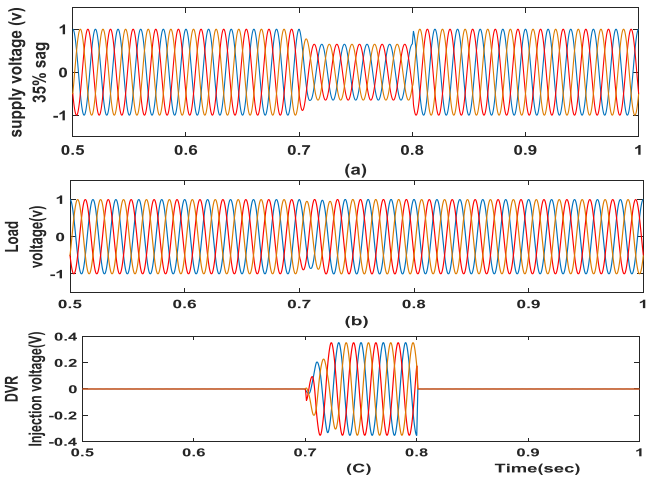
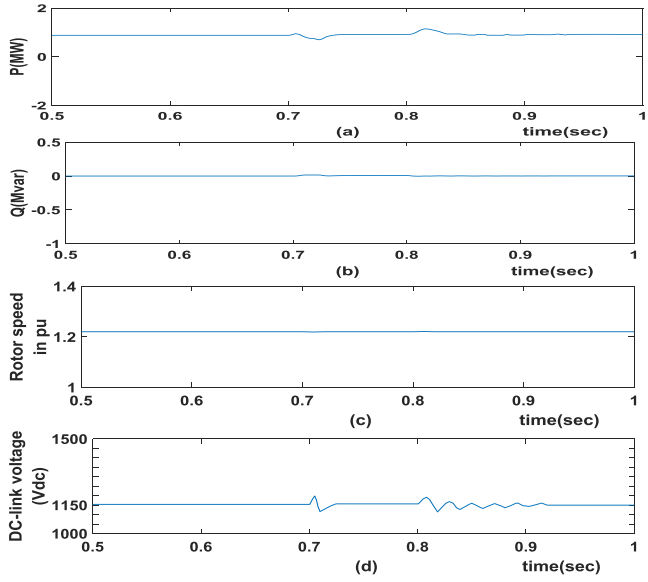


Fig. 8. the results of DVR using FLC-CFFFB control for 0.35 pu of balanced sag condition.

Under fault condition, the DFIG injects the active power is almost zero. But use of DVR, the DFIG-WT maintained the active power generation at 1.5 MW and provide smooth real power during fault condition shows in Fig 9(a) and also the reactive power support by the DVR to the DFIG-WT shows in Fig 9(b). the DVR injects the drop voltage during faults to keep constant terminal voltage of DFIG. In Fig 9(c) shown speed control of rotor and threshold value of rotor speed is 1.2. Dc-link voltage shows in Fig 9(d), It is not more than threshold value. Fig 9(e) and 9(f) shows currents of stator and rotor respectively under faults conditions and they are with in threshold values. this simulation results shows that during fault conditions DVR work efficiently to reduce the transient voltage and currents in DFIG.

B. CASE 2: 35% UNBALANCED SAG

Operation of DFIG-WT using DVR is analyzed during Single line to ground faults condition of unbalanced sag from 0.7s to 0.8s of supply voltage shows in Fig 10(a) and it is compensated using DVR with CFFFB control to maintain constant load voltage shows in Fig 10(b). Fig 10(c) shown injected voltage of DVR in volts.



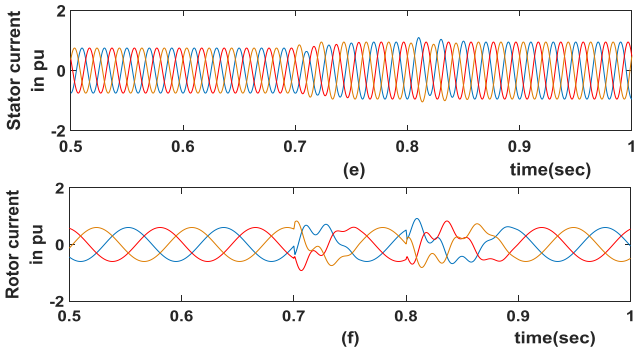


Fig 9: The results of balanced sag between 0.7s to 0.8s using FLC-CFFFB of DVR for FRT capability. (a) Active power in pu. (b) Reactive Power in pu. (c) Rotor speed in pu. (d) DC-link voltage in volts. (e) Stator current in pu. (f) Rotor current in pu.

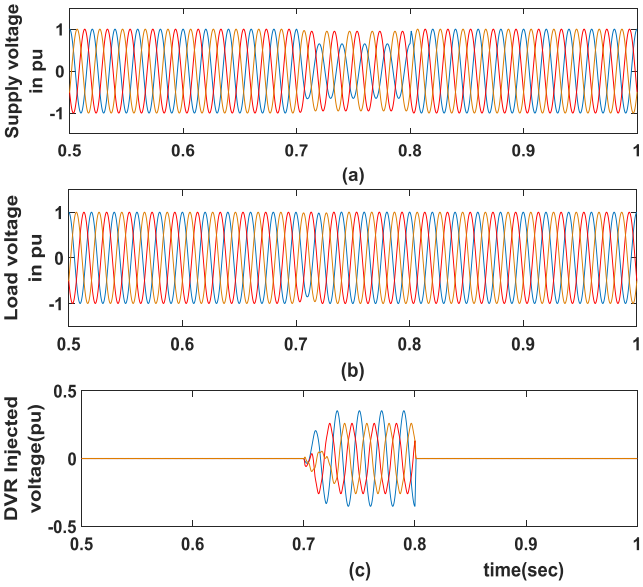
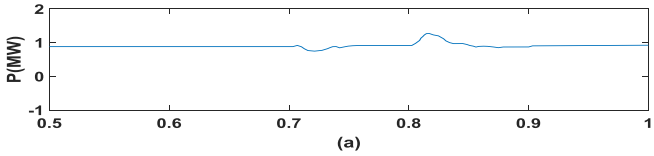


Fig. 10. The results of DVR using FLC-CFFFB control for unbalanced condition.

When grid fault occurs, the DFIG supply the active power is almost zero. this leads to stress on mechanical system. At that instant, the DFIG-WT has capable to send the real power using DVR to grid shown in Fig 11(a). there by the DFIG is keep the active power at 1.5 MW and provide smooth power generation even under fault conditions and also supplying reactive power using DVR shown in Fig 11(b). Improvement of FRT capability is important to maintain stability under fault condition. During fault condition, stator and rotor currents increased at that time RSC controlled real and reactive power separately and maintain rotor speed at 1.2 pu shown in Fig 11(c). Fig 11(d) shown DC-link voltage value below threshold limits of 1.35 pu. DVR reduces higher currents to protect the rotor and continue to its operation. The currents of stator and rotor values are well under threshold limits shows in Fig 11(e) and 11(f) and it takes at least 4 cycles to get stable condition.



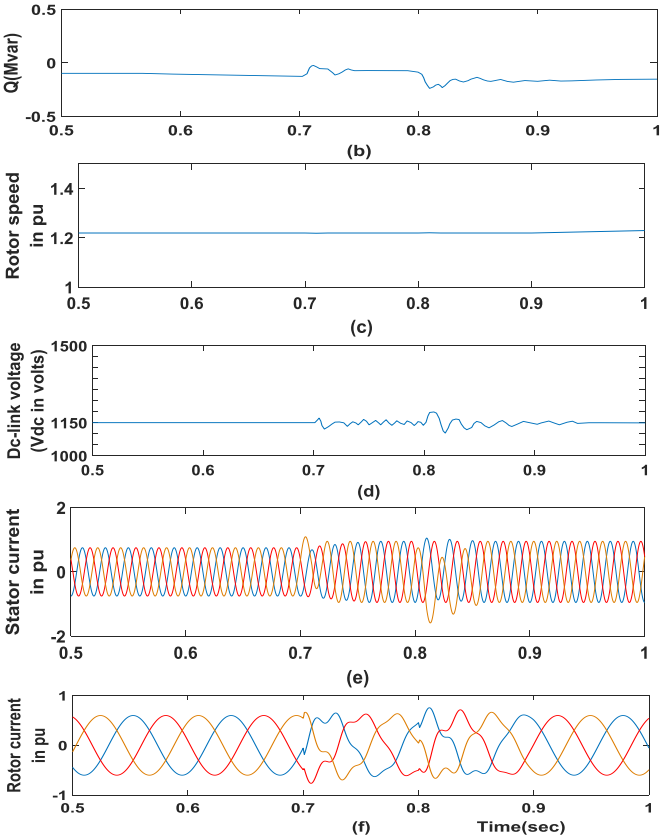


Fig 11: The results of Unbalanced sag between 0.7s to 0.8s using FLC-CFFFB of DVR for FRT capability. (a) Active power in pu. (b) Reactive Power in pu. (c) Rotor speed in pu. (d) DC-link voltage in volts. (e) Stator current in pu. (f) Rotor current in pu.

C.CASE 3: SHORT-CIRCUIT FAULT (3LG FAULT)

The operation of DFIG-WT using DVR is analyzed during short circuit condition between 0.7s and 0.8s. The supply voltage under short circuit condition is shown in Fig 12(a) and voltage drop compensated by using DVR with CFFFB control to maintain constant load voltage shows in Fig 12(b). Fig 12(c) shows injected voltage of DVR.

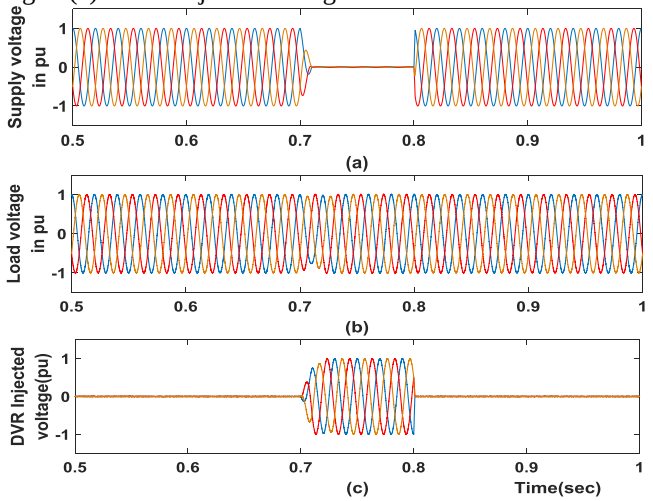


Fig. 12. the results of DVR using FLC-CFFFB control for short circuit condition.

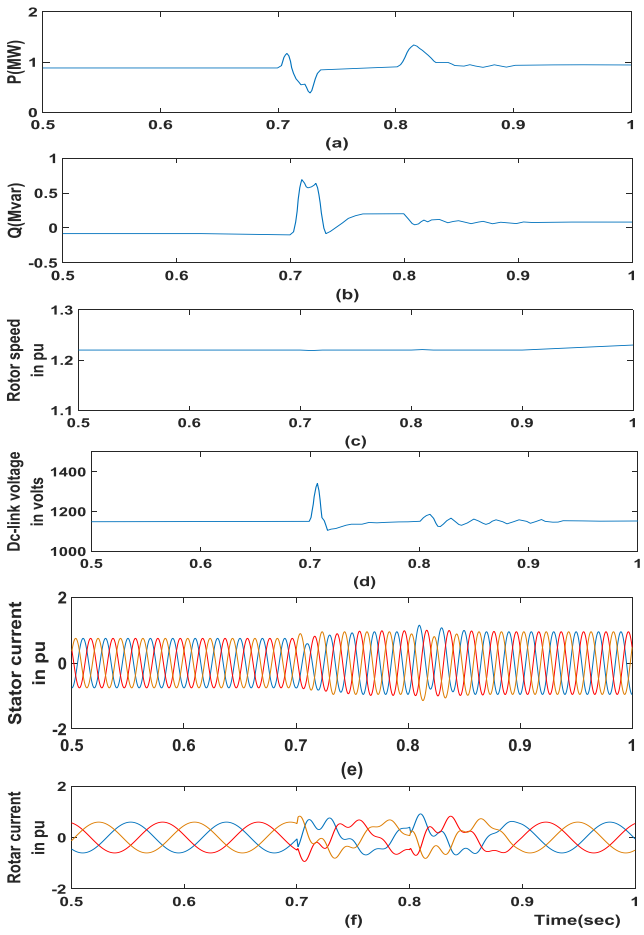


Fig 13: The results of DVR using FLC-CFFFB control for short circuit condition between 0.7s to 0.8s. (a) Active power in pu. (b) Reactive Power in pu. (c) Rotor speed in pu. (d) DC-link voltage in volts. (e) Stator current in pu. (f) Rotor current in pu.

During fault conditions the real power reduces but the DFIG takes the DVR help to balance the real power shows in Fig 13(a) and also the DFIG gives reactive power to grid to continue its operation using DVR shows in Fig 13(b). DVR supply voltage using VSC through LC type filters and coupling transformer to correct the faulty line voltages. Therefore, control structure of DVR is does not change during fault conditions and moreover it accept the real and reactive power supporting to grid under faults.

The CFFFB is a combination of FLC based feed-back and feed-forward control. FLC is used to get the deviation voltage and that required voltage is compensated using DVR. Due to the sudden drop voltage in short circuit condition, the Dc-link shows sudden peak value in Fig 13(d) but the voltage value is present under threshold value at 1.35 pu. The stator and rotor currents values also present below the threshold values shows in Fig 13(e) and 13(f). When DVR is removed, the stator and rotor currents oscillate and it takes at least 4 cycles to get normal values and these results shows enhancement of FRT capability using DVR with FLC based CFFFB during fault conditions in DFIG-WT. Among the fault conditions, short circuit condition is poor and it depends more on DVR. DVR and DFIG simulation parameters shown in table 2.

Table 3: Comparison of harmonic mitigation using PI and FLC of DVR

% THD values	DVR load voltage with PI based CFFFB	DVR load voltage with FUZZY based CFFFB
35% Balanced sag	6.61%	2.74%
35% Unbalanced sag	6.63%	2.76%
Short circuit fault	14.96%	4.63%

D. CASE 4: HARMONICS SPECTRUM ANALYSIS

When grid fault occurs, the harmonics shows more negative impact on the grid. To reduce the harmonics in the DFIG-WT, the operation of DVR is analyzed based on various controllers. the hormonic mitigation using DVR with PI controller is shows in Fig 14 and the hormonic mitigation using DVR with FLC controller is shows Fig 15. From Fig 14 and Fig 15 we conclude that the DVR with FLC shown %THD values below the IEEE 519 standards. Table 3 shows the exceptional development in DVR operation with help of FLC-CFFFB control.

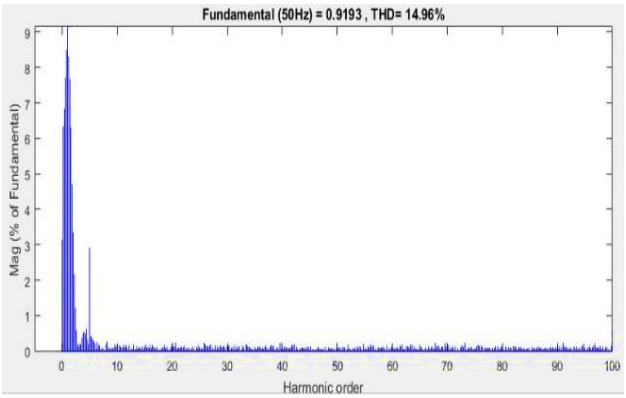


Fig. 14. Harmonic spectrum shows THD 14.96 % of Load voltage using DVR with PI-CFFFB during short circuit condition.

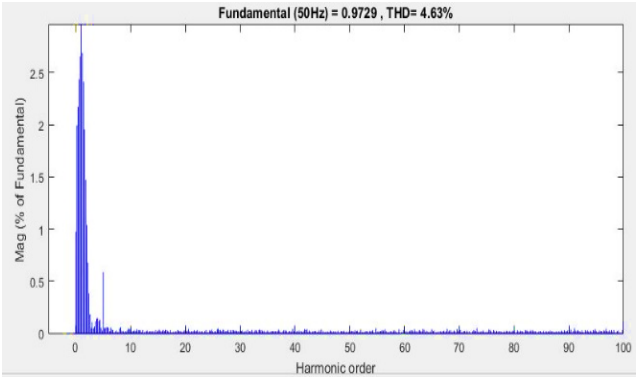


Fig. 15. Harmonic spectrum shows THD 4.63% of Load voltage using DVR with FLC-CFFFB during short circuit condition.

From the results and discussion shows that betterment in load voltage, rotor and stator currents, Dc-link balancing in DFIG-WT under faults condition are obtained. When grid fault occurs the DFIG-WT deliver 1.5 MW of smooth active power with minor oscillations using DVR is observed and also observed better reactive power support under faults.

DVR reduce harmonic distortion during fault condition using FLC based CFFFB control. In terms of percentage THD values, the performance of both controllers is observed and found that FLC-CFFFB of DVR provides the lesser harmonic disturbance.

V.CONCLUSION

This paper investigates the enhancement of FRT capability using FLC-CFFFB of DVR in DFIG based WT. The operation of the PI and FLC is compared in DVR for the voltage sag mitigation, smooth real power, reactive power support and current control during transient conditions. As per IEEE standards, comparison of two controllers in terms of percentage THD shown that using FLC-CFFFB of DVR provides good harmonic compensation and simulation results show that DVR is well-suited for enhanced FRT capability in DFIG-WT.

REFERENCES

1. R. A. J. Amalorpavaraj, K. Palanisamy, S. Umashankar, and V.K Ramachandramurthy, (2017). "Improved fault ride through capability in DFIG based wind turbines using dynamic voltage restorer with combined feed-forward and feed-back control". *IEEE Access*, *5*, 20494-20503
2. D. Hansen and G. Michalke, ''Fault ride-through capability of DFIG wind turbines,'' *Renew. Energy*, vol. 32, no. 9, pp. 1594–1610, Jul. 2007.
3. C.Feltes, Wrede, H., Koch, F. W., & Erlich, I. "Enhanced fault ride-through method for wind farms connected to the grid through VSC-based HVDC transmission". *IEEE Transactions on Power Systems*, *24*(3), 1537-1546, Aug. 2009.
4. B. B. Ambati, P. Kanjiya, and V. Khadkikar, ''A low component count series voltage compensation scheme for DFIG WTs to enhance fault ride-through capability,'' *IEEE Trans. Energy Convers.*, vol. 30, no. 1, pp. 208–217, Mar. 2015.
5. A. O. Ibrahim, T. H. Nguyen, D. C. Lee, and S. C. Kim, ``A fault ride through technique of DFIG wind turbine systems using dynamic voltage restorers," *IEEE Trans. Energy Convers.*, vol. 26, no. 3, pp. 871_882, Sep. 2011.
6. M. Farhadi-Kangarlu, E. Babaei, and F. Blaabjerg, ''A comprehensive review of dynamic voltage restorers,'' *Int. J. Electr. Power, Energy Syst.*, vol. 30, no. 92, pp. 136–155, Nov. 2017.
7. R. A. J. Amalorpavaraj, P. Kaliannan, and U. Subramaniam, ''Testing of low voltage ride through capability compliance of wind turbines—A review,'' *Int. J. Ambient Energy*, vol. 39, p. 120, Jul. 2017.

AUTHORS PROFILE

SIDDU BALARAMI REDDY has graduated his B.Tech from Y.S.R Engineering college of Y.V.U, Proddatur, A.P, India and currently he is pursuing M.Tech (EPS) from JNTUA college of Engineering and technology, Ananthapuramu-515003, A.P, India.

M. RAMASEKHARA REDDY has graduated his B. Tech from M.S. Bidve Engineering college, Latur in 1999, M.H, India and M. Tech from JNTUA College of Engineering, Ananthapuramu in 2007, AP. Presently he is the assistant professor in electrical engineering from the JNTUA College of Engineering, anantapuramu, AP, India.