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Leakage Power Minimization using IVC based GSA

P. Indira, M. Kamaraju, Ved Vyas Dwivedi

Abstract*: The power management has become the major constraint while designing VLSI circuits as parameters like Area, Speed, etc. are critical to be optimized. In this work, a low power 16-bit ALU is designed to perform all arithmetic and logic operations. The present day super computers, mobile gadgets, calculators etc. are using low power ALU systems to perform their tasks. Especially, leakage power occupies major portion of power consumption in the CMOS circuits, as the process technology progresses. The objective of the research work is to reduce leakage power in maximum extent to run the ALU with low power. The proposed model has used IVC based leakage power reduction technique in standby mode by using Gravitational Search Algorithm (GSA). Input Vector Control (IVC) technique is found to be a better alternative in achieving low leakage as it is based on the effect of transistor stacking and it is highly preferred because of its independency over other technological parameters without performance overhead. The GSA locates MLV (Minimum Leakage Vector) in vector combinations of input test circuits of ALU. And then IVC forces the other vector combinations into MLV mode of a test circuit to reduce leakage power. The comparison study has been carried out with Genetic Algorithm (GA) and Particle Swarm Optimization (PSO) algorithm with various test circuits. Power analysis is conducted with GSA to ascertain better leakage reduction and also it locates MLV in less number of iterations. GSA takes only 13 iterations to reach its global space, whereas, PSO takes 62 iterations and GA takes 96 iterations to reach their global space. The simulations are carried out using the Xilinx platform with Verilog coding using PSPICE and MATLAB tools.

***Keywords:** Input Vector Control, GSA, GA, PSO, MLV.*

I. INTRODUCTION

In Deep sub-micron technology, power has turned to be the most important factor in VLSI system design. With recent developments and demands of customers, designers and researchers are trying to fulfill the needs of the present day requirements, such as multi-tasking, parallel operations, high speed [1], etc. In addition to it Area (compactness), Cost, Performance, Reliability are also major constrains in VLSI system design and they all need more power consumption.

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Hence, low power techniques are very much needed, while designing the VLSI circuits, to fulfil the above constraints.

Leakage power is progressively place a vital role in low power VLSI design. Leakages in VLSI circuits depend mostly on Scaling and Transistor count. As more advanced features are added in the VLSI design, the transistor count on chip increases accordingly, leading to more leakage power. Leakage power predominantly changes its scenario as it dominates dynamic power as process technology progresses to 65 nm, because it has increased from 30 to 50% of the total IC power utilization. According to International Technology Road map for Semiconductors (ITRS), for any optimal design, leakage power control is very much desirable; so designers must emphasize on this factor and apply various minimization techniques to reduce it [2][3]. Most of the battery operated devices require more power. During idle mode, most of the power is drained very quickly due to leakages in CMOS circuits. Those are source/drain junction leakage current, gate direct tunneling leakage, sub threshold leakage current through the channel of an OFF transistor. Among the above leakage currents in CMOS technologies, the major portion of leakage arise with sub-threshold leakage current [4]

Different approaches and techniques are considered to reduce the leakage power. One good technique is 'Input vector control', which is not dependent on process technology and it is built on transistor stacking that gives awful reduction in leakage power without compromising to its performance [5][6].

There are several algorithms used in this aspect to locate the minimum leakage vector (MLV) of test circuits to minimize leakage power. These heuristic search algorithms are genetic algorithm, particle swarm optimization algorithm, linear search algorithm, fast heuristic algorithm, etc.

Genetic algorithm is used with input vector control method and developed test patterns to evaluate the design in terms of minimum leakage power [7]. The minimum leakage vector is optimized with fitness function as Circuit Status Difference (CSD) to achieve better leakage power reduction with run time [8].

Particle Swarm Optimization (PSO) algorithm has been deployed in the field of Low Power VLSI circuits to evaluate the key parameters such as area, delay and power consumption, in designing single bit full subtractor with different process technologies [9]. The study used BS1M4 parameter tool for the analysis and the results obtained with 90 nm technology are better when compared to other conventional full subtractor methods.

In this work, another optimization algorithm called GSA is employed for tracing the minimum leakage vector. The leakage powers for all input combinations of test circuits are obtained by using PSPICE tool and specially designed ALU model is analyzed for the purpose of power saving.

The organization of the paper is as follows:

The importance of the leakage power and the sources of the leakage power with various algorithms associated to reduce leakage power is described in Introduction Section-I. The Problem statement or Objectives, scope of the paper and Problem Methodology with System Model are presented with a block diagram in Section-II. Specially designed ALU with test circuit construction is illustrated in Section-III. Section IV describes the previous algorithms which are worked with the same IVC technique to reduce leakage power. Section V is about the theoretical background of Gravitational Search Algorithm. Section VI envisages the importance of the leakage power in motivation. By taking 3-bit test circuits (AND and ADD) in Section VII, leakage power reduction analysis is carried out. In Results and Comparative section (Section-VIII), GSA results are compared with other Algorithms and found better results in terms of leakage power reduction and the time required to locate minimum leakage vector. Finally, Sections IX and X present the Conclusion followed by Limitations and Future Scope of this design.

II. PROBLEM METHODOLOGY

The proposed work is to design a Low power 16-bit ALU model using PSPICE tool. A basic arithmetic and logic unit is designed to perform all the mathematical and bit manipulation operations as per the requirement of the customer.

The basic objective of this work is to reduce leakage power with specially designed ALU model test circuits. For effective reduction of leakage power, GSA is used.

Minimum leakage vector (MLV) is identified by using gravitational search algorithm. The worst case and the best case of test circuit in input combinations were identified. Based on the best case, i.e., least leakage state, all other input combinations of test circuits are forced into the minimum leakage state so as to reduce the total leakage power.

The Single-input test circuits are constructed using PSPICE tool. Based on that, 2-input, 4-Input, 6-Input, 8-Input and 10-Input NAND gate test circuits are constructed for comparison. Similarly, 16-bit ALU is designed and various operations are performed with different test circuits that are explained in the following sections.

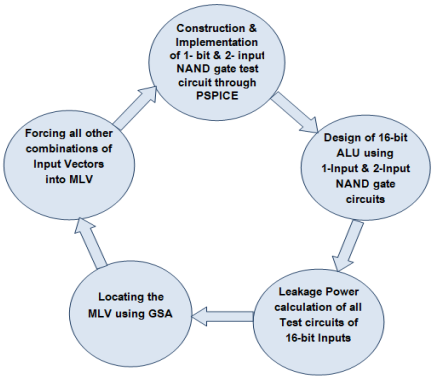

Fig. 1. Leakage Power Reduction System Model

The above block diagram explains the methodology, how the leakage power is reduced with the use of Low Power Test circuits of ALU model.

In this paper, maximum 16-bit test circuits are constructed to design a Low Leakage ALU Model. Further, 32-bit, 64-bit test circuits can be constructed in the same way.

III. ARITHMETIC AND LOGICAL UNIT (ALU)

Arithmetic and Logic Unit (ALU) is the brain of the processor, which performs various operations. A simple 16-bit ALU block diagram is represented below.

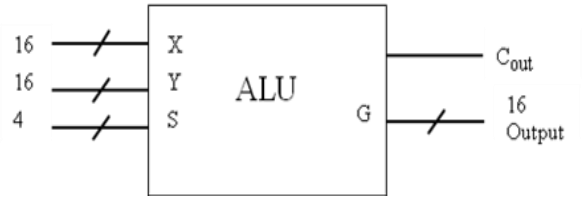

Fig. 2. 16-bit ALU Block diagram

This ALU is designed with 4 selection lines and the truth table would have $2^4 = 16$ input combinations. We encapsulate the complete circuit in a "black box" so as to reuse for any number of bits.

Here, 'X' represents the Arithmetic Unit, where 16-bit Arithmetic operations are performed like ADD, SUB, INC, DEC, etc. Here C_{in} is also included in 'X' to produce C_{out} for addition operation and borrow for subtraction operation.

'Y' represents the logical unit, where bit-wise operations are performed with individual 16-bit test circuits of AND, OR, XOR, XNOR, NAND, NOR, etc.

'S' represents the 4-bit select lines (S_0 S_1 S_2 S_3) to select the operations, whether it could be arithmetic (or) logical, that are performed as shown in Table 1. It is used as a control signal that selects the specific operation to be performed. G represents the 16-bit output, which depends upon the operation selected.

Table I. Operations of ALU

OPCODE				OPERATIONS
S_0	S_1	S_2	S_3	
0	0	0	0	Clear (Default output '0'
0	0	0	1	ADDITION
0	0	1	0	ADDITION with CARRY
0	0	1	1	SUBTRACTION
0	1	0	0	SUB with Borrow
0	1	0	1	AND
0	1	1	0	OR
0	1	1	1	XOR
1	0	0	0	NOT (complement)
1	0	0	1	NAND
1	0	1	0	NOR
1	0	1	1	XNOR
1	1	0	0	Buffer (same as Input)
1	1	0	1	INC
1	1	1	0	DEC
1	1	1	1	Set to all 1's

A. Test Circuit Design

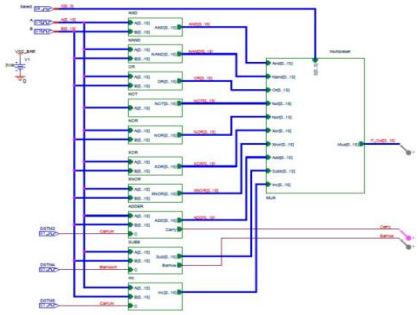

Fig. 3. Test circuits representation in ALU Model.

The congregation of all the test circuits in ALU model is represented in Fig. 3. Simulation and calculation of leakage powers of test circuits are carried out using PSPICE tool.

At first, a single bit NAND gate structure is formed by using CMOS transistors. The 16-bit test circuits are framed by using the sub-module of this single bit NAND gate structure. The other test circuits are also designed in the same way to form this ALU model.

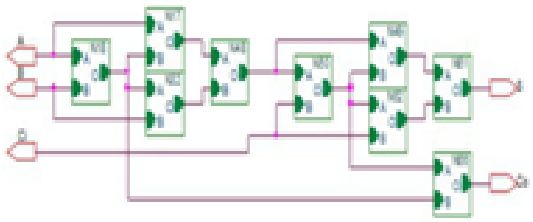

Fig. 4. 1-bit Full Adder Using NAND Gate

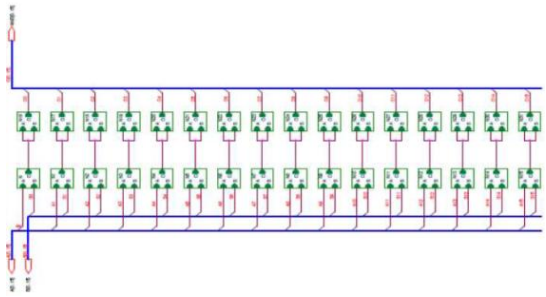

Fig. 5. 16-bit ALU AND operation.

The designs of individual test circuits are presented here in Fig. 5 to Fig. 12. All the circuits are integrated to form a single ALU model. The operations are controlled by providing opcode to the multiplexer.

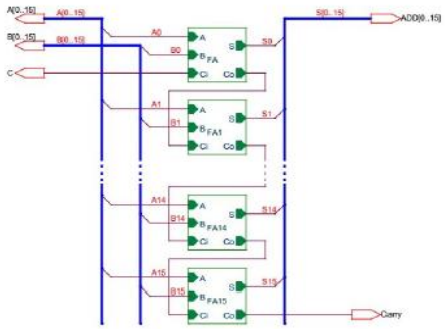

Fig. 6. 16-bit ALU Addition Operation.

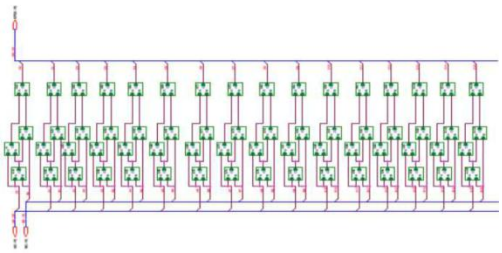

Fig. 7. 16-bit ALU XOR Operation.

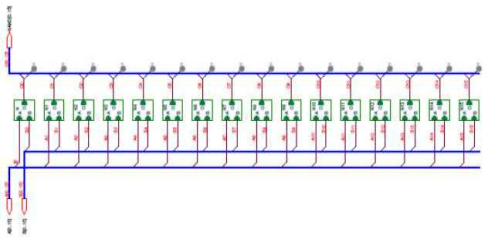

Fig. 8. 16-bit ALU NAND Operation.

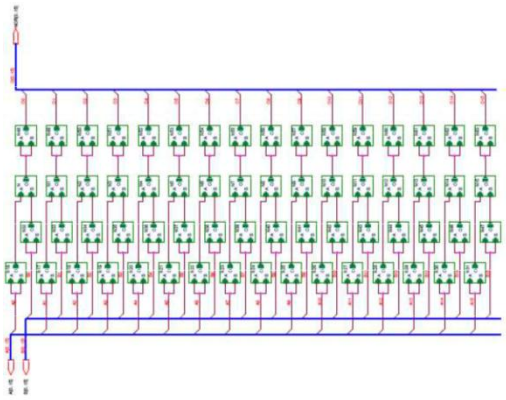

Fig. 9. 16-bit ALU NOR Operation.

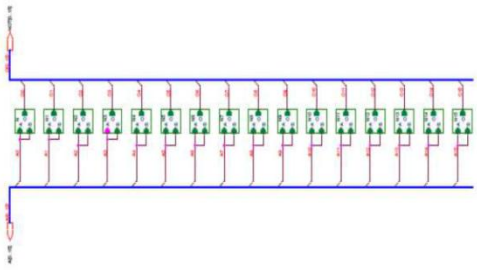

Fig. 10. 16-bit ALU NOT Operation.

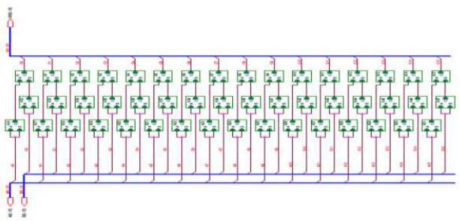

Fig. 11. 16-bit ALU SUB Operation.

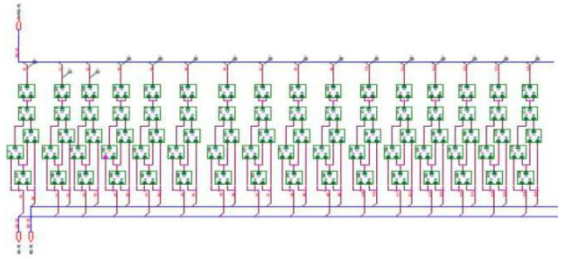

Fig. 12. 16-bit ALU XNOR Operation.

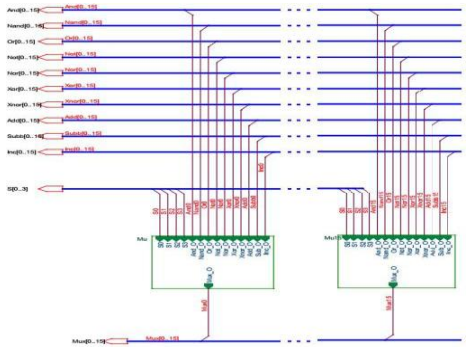

Fig. 13. 16-bit ALU Multiplexer Operation.

Fig. 4 shows the block diagram of 1 bit NAND gate and the same is used as a base model for the ALU and selected as sub module. By using the same sub module, the main ALU module is developed as shown in Fig. 5, 6, 7, 8, 9, 10, 11 and 12, which contain 16-bit AND, ADD, XOR, NAND, NOR, NOT, SUB and XNOR test circuits respectively. In the similar process, the Mux module is also developed to integrate the designed sub modules into a 16 bit ALU circuit and is further processed to calculate the leakage power of the circuit.

IV. PREVIOUS WORK

A. Genetic Algorithm (GA):

A genetic algorithm is a metaheuristic algorithm used in computing and to find true (or) approximate solutions for optimization and search problems, based upon the algorithm termination. It is based on the important issues in Biology, such as mutation, cross over, inheritance and selection. The key elements of GA are chromosomes or genotypes or phenotypes, which are used in computer simulations where in the generations, are produced. The better generations will be evolved by combining the key elements to achieve optimal solution.

Genetic Algorithm steps:

Genetic Algorithm is used to reach the global space, i.e., to find the minimum leakage vector of various test circuits to reduce the leakage power.

- Choose the initial population, i.e., all combinations of 3-input test circuits.
- Compute leakage power for all input combinations.
- Determine the fitness function for each vector in the swarm.
- Use various heterogeneous methods of selection, crossover, mutation to find out the best case, i.e., minimum leakage power vector.
- Declare the optimal solution as MLV.

B. Particle Swarm Optimization (PSO) Algorithm:

Particle Swarm Optimization is an advanced search algorithm and it best suits to Non-linear problems. It is not a random search technique, as the particles in the population move according to their previous best position and their velocities. Each particle compares its present position with the other particle's better position and moves towards final best position. Same way, all other particles also move towards final best position. That position is called Global Best Position (g(t)).

Similarly, each particle moves in a global space to reach its goal. Those movements are called as iterations. How best each particle attains its goal depends on its number of iterations. More number of iterations means the particle needs more time to reach its final position.

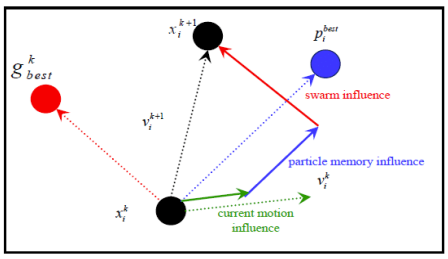

Fig. 14. PSO representation

Fig. 14 represents the graphical model of PSO where the current position of particle is $X_i(t)$ and the velocity is $V_i(t)$. With the influence of swarm, 'i' particle moves towards its local best and global best positions.

V. GRAVITATIONAL SEARCH ALGORITHM (GSA)

GSA is a swarm intelligence search algorithm. In the gravitational global space, the masses (heavier/ lighter) are inclined to move towards each other. As per the Newton's law of gravity, "Each particle attracts every other particle with a gravitational force. The gravitational force between two particles is directly proportional to the product of their masses and inversely proportional to the square of the distance between them".

$$F = G\frac{M_1 M_2}{R^2}$$

"F = magnitude of gravitational force
G= gravitational constant
M_1, M_2 = the mass of the first and second particles
R = the distance between the two particles"

Acceleration (a) is defined in terms of force and mass of the particle as,

$$a = \frac{F}{M}$$

$$F_{ij} = G\frac{M_{aj} M_{pi}}{R^2}$$

$$a_i = \frac{F_{ij}}{M_{ii}}$$

"M_{aj} = Active gravitational mass of object j
M_{pi} = passive gravitational mass of object i
M_{ii} = inertia mass of object i"

Every object accelerates towards the resultant force that acts on it from the other objects. The lighter mases move quickly in the gravitational space when compared to the heavier ones and merges into heavier masses. Thus, they converge into one global solution.

The procedure for developing gravitational search algorithm is as follows,

- Recognition of search space
- Derivation of initial population
- Evaluation of fitness function for every individual population
- Regularly update the gravitational fitness function value

Let us consider an object with 'M' masses. The position of the nth agent is given by,

$$Xn = \{X_n^1, \ldots\ldots\ldots\ldots, X_n^d, \ldots\ldots\ldots\ldots X_n^1\}$$

where, n=1, 2,……M;

X_n^d represents the position of nth agent in the dimension d.

For a particular period of time, the force acting on the mass 'n' from the mass 'k' is given by,

$$F_{nk}^d(t) = G(t)\frac{M_{pn}(t)*M_{ak}(t)}{R_{nk}(t)+\epsilon} * \left(x_k^d(t) - x_n^d(t)\right)$$

where,

"M_{ak} = active gravitational mass with respect to agent 'k'.

M_{pn} = Passive gravitational mass with respect to 'n'

G(t) = gravitational constant.

'ϵ' = small constant.

$R_{nk}(t)$ =Euclidean distance amongst the agents 'n' & 'k'".

Further, to apply stochastic character to the developed algorithm, it is assumed that the entire force acting on the agent 'n' in a dimension 'd' is a random weighted sum of dth components with forces exerted from other agents which is given by,

$$F_n^d(t) = \sum_{k=1,k\neq n}^{M} Rand_k . F_{nk}^d(t)$$

where, the random number is given through Rand$_k$ with the limit [0,1].

Furthermore, the inertial mass and the gravitational mass are calculated through the fitness evaluation step. More efficient results can be obtained through higher mass values. By assuming the values of equality of inertial and gravitational masses, individual mass values are calculated through the fitness map which is given by,

$$m_n(t) = \frac{fitness_n(t) - Worst_{case(t)}}{Best_{Case(t)} - Worst_{case(t)}}$$

$$M_n(t) = \frac{m_n(t)}{\sum_{k=1}^{M} m_k} \qquad (5)$$

Optimal function can be achieved with number of iterations until it reaches its global solution.

VI. MOTIVATION

Previously, dynamic power conservation is the highest priority in Low Power VLSI design, as it consumes 90% of the total power. The leakage power prominence increases as the process technology is moving towards thinner nano technology. It is depending on many more factors like, Circuit geometry, Temperature, Doping and Processing. It is becoming complicated and worthy of being controlled. Otherwise, one can meet all complex features but the VLSI design is prone to vulnerability. Finally it endangers the circuit performance.

Now, the scenario has changed and designers are moving towards 180 nm to 90 nm technology and further to 65 nm technology, which greatly increased the burden of static power. Based on ITRS report, sub threshold leakage power dominates the dynamic power in 65 nm size chip.

There are several techniques available for leakage power reduction in active mode. But, in this work, we want to control the leakage power in standby mode. In the battery operated devices, power gets wasted by means of leakages, as it drains out in idle mode. Hence one must identify such leakages and find the ways to minimize.

VII. LEAKAGE POWER ANALYSIS

In this work, leakage power analysis is carried out by using 3-input AND rate and ADDITION gate with the test circuits by considering all input combinations of leakage powers. Gravitational search algorithm locates the Minimum leakage state. By using IVC method, leakage powers of all other combinations of test circuits are reduced with respect to MLV.

Table II describes the AND operation with AND test circuit. All the input vector combinations of leakage powers are measured using MATLAB tool. Among them, 001 input combination is having lowest leakage power (2.4538 nW), and hence, it is the minimum leakage vector (MLV). It is considered as the best case and all the other input vectors are forced into this state to minimize the Total leakage power. In this, the worst case is the highest leakage state which is placed with 011 input combination.

TABLE II. 3-Input AND Operation for Leakage Power estimation using GSA

Select Line	ABC	Leakage Power (W)
0101	000	3.7521n
	001	2.4538n (best)
	010	27.339m
	011	26.544m (worst)
	100	18.318m
	101	18.107m
	110	16.902m
	111	16.876m

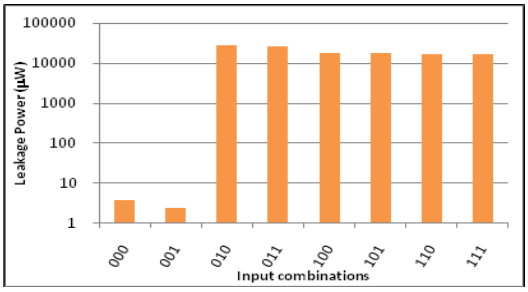

Fig. 15. Leakage powers for AND operation.

The above graph plotted between input vector combinations with leakage power consumption in logarithmic scale. The least leakage power is in nano-watts range and highest leakage is in micro-watts range and the difference is very high. According to IVC technique, that much power is chopped off.

TABLE III: 3-Input ADDITION operation for Leakage Power estimation using GSA

Select Line	ABC	Leakage Power (W)
0001	000	3.1632n
	001	2.7189n (best case)
	010	27.242m (worst case)
	011	26.873m
	100	18.209m
	101	18.117m
	110	15.863m
	111	15.956m

Table III displays all the 3-input test circuit combinations of ADDITION operation. The least leakage vector identified is '001' input combination. And the highest leakage power consumption corresponds to the input combination of '010'.

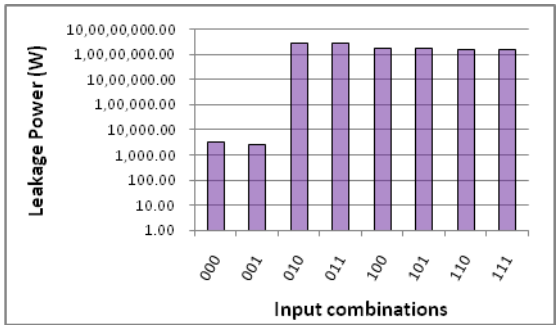

Fig. 16. Leakage powers for ADDITION operation.

The above figure shows the leakage powers consumed with different input vectors for three input–ADDITION operation. The difference between highest and lowest leakage vectors is in the range of 92%.

The average power consumption of 3-input NAND gate of all input combinations is 1.5027E-05; and the minimum leakage power consumption is 2.0255E-09.

P_{saving} (%) = (1–minimum leakage power / Average leakage power)* 100

Here, by using IVC based GSA model, 99.98% of leakage power is saved; that means only 0.002% of power is being wasted, shown in Table-IV.

For the rest of the test circuits, average leakage power and minimum leakage power of all input combinations are calculated and tabulated in Table IV and Individual leakage powers or other circuits are not tabulated here due to space constraint.

TABLE IV. Percentage of Power saved of 3-Input Test Circuits

Operation	Selection Line	Average Leakage Power (W)	Minimum Leakage Power (W)	% Power saved
Clear (Default output "0")	0000	1.22E-05	5.01E-10	99.9959
ADDITION	0001	1.53E-05	2.72E-09	99.9822
ADDITION with CARRY	0010	1.59E-05	7.97E-10	99.9950
SUBTRACTION	0011	1.46E-05	2.81E-09	99.9807
SUB with borrow	0100	1.50E-05	5.88E-10	99.9961
AND	0101	1.55E-05	2.45E-09	99.9842
OR	0110	1.53E-05	6.09E-10	99.9960
XOR	0111	1.49E-05	1.67E-09	99.9888
NOT (complement)	1000	1.51E-05	4.74E-10	99.9969
NAND	1001	1.50E-05	2.03E-09	99.9865
NOR	1010	1.57E-05	8.08E-10	99.9949
XNOR	1011	1.50E-05	3.21E-09	99.9786
Buffer (same as Input)	1100	1.51E-05	5.25E-10	99.9965
INC	1101	1.54E-05	1.30E-09	99.9916
DEC	1110	1.49E-05	4.71E-10	99.9968
Set to all 1's	1111	1.53E-05	2.19E-09	99.9857

In the above table, the different selection lines select different test circuits according to the ALU design; and by considering the different input combinations of leakage vectors, average leakage powers and minimum leakage powers are calculated and obtained the percentage of power saving and the values are graphically represented as below:

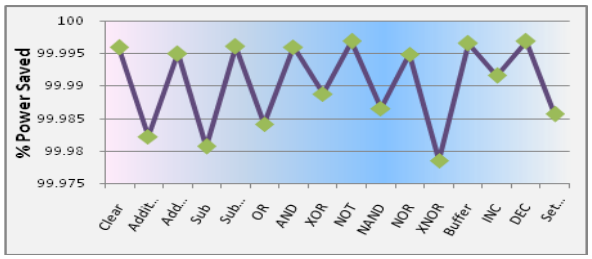

Fig. 17. 3-bit Circuits Power Saving using IVC based GSA.

From the above figure, whatever is the test circuit, the power saved is almost 99% (saved through the input vector control based GSA algorithm).

A. Leakage Power Analysis with time varying graph

Leakage power is analyzed with 16-bit data input of X and Y is carried out with PSPICE platform shown in Fig. 14 and Fig. 15. The simulation output of 16-bit data of AND operation is shown in Fig. 16. Fig. 17 shows the Leakage Power analysis obtained with Time varying graph.

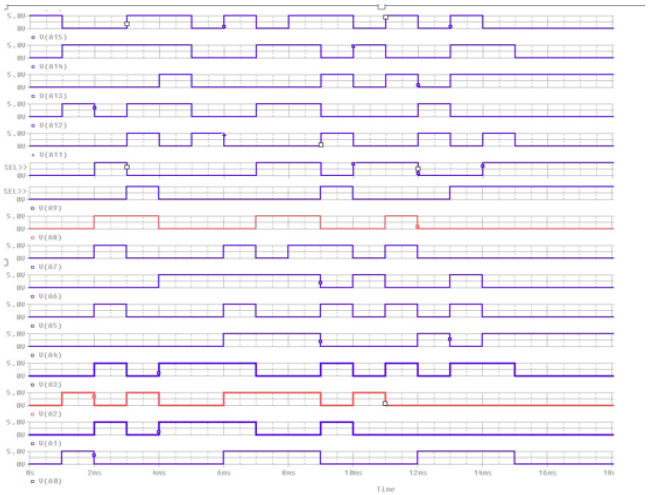

Fig. 18. X-input of 16-bit data

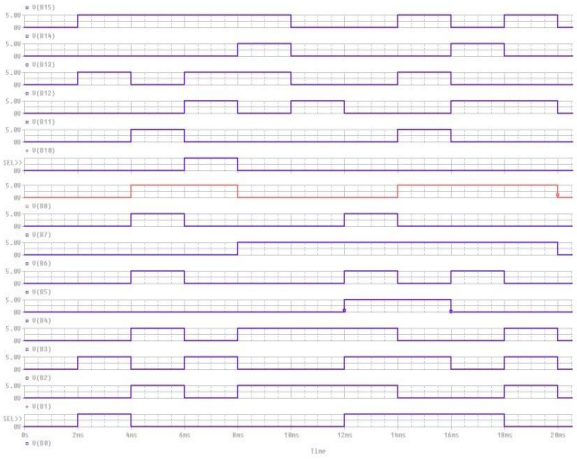

Fig. 19. Y-input of 16-bit data

Fig. 20. 16-bit data Output

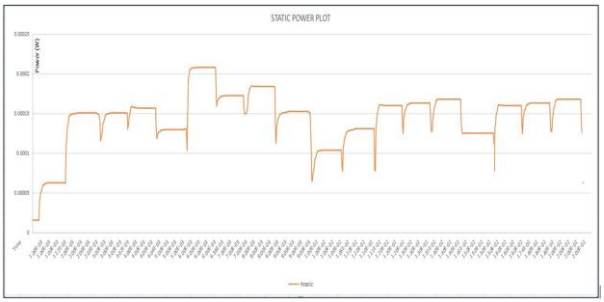

Fig. 21. Leakage Power Analysis vs. Time plot.

Table V. MLP with GSA with AND 16-bit test circuit

Test Circuit	Input Vector	MLP with GSA (pico watts)
AND	X = 0110111001000110 Y = 0110011100100110	20.13

Table V contains the results acquired from the 16-bit AND test circuit of ALU. The leakage power analysis is carried out with random X, Y vector input combinations of data as shown in Fig. 21. Gravitational Search Algorithm is employed for the test circuit inputs and the minimum leakage power is determined. The MLP achieved with AND test circuit is 20.13pW with input vectors of X=0110111001000110 and Y = 0110011100100110, as indicated in the above table. Hence, X and Y are the minimum leakage vectors determined by GSA. Moreover, the optimal iteration is achieved through GSA is at 16.

VIII. RESULTS AND COMPARATIVE ANALYSIS

By using Verilog HDL coding, minimum leakage vector (MLV) is identified through Gravitational Search Algorithm. Xilinx 9.2i tool and PSPICE tool are used in this regard to determine leakage power. Based on those leakage powers of different test circuits and input vector combinations, MLV is determined.

Genetic Algorithm and Particle Swarm Optimization simulations are carried out in H-spice tool for calculating overall leakage power and MLV. The results are checked by CADANCE tool. The G_{best} value with minimum leakage power is further processed with PSPICE simulation platform for calculating the total leakage power.

Input Vector control is the best technique to minimize the leakage power by using the minimum leakage vector. It does not depend on process parameters and it considers only stacking effect. For a set of input vectors, leakage powers are measured. And then, MLV can be identified with different Algorithm techniques. Subsequently, IVC forces all other input vectors of test circuit to MLV in standby mode to minimize the leakage power.

TABLE VI. Results obtained from GSA algorithm for different test circuits

Test Circuit	Population Size	MLV	No. of iterations	Leakage Power (pW)
C17 Benchmark circuit	8	00101	1	28.56
	20		1	
	30		1	
	50		1	
4 Input circuit	8	000000	1	10.79
	20		1	
	30		1	
	50		1	
6 Input circuit	8	000000	1	21.58
	20		1	
	30		1	
	50		1	
8 Input Circuit	8	00000000	15	21.735
	20		7	
	30		2	
	50		2	
10 Input circuit	8	0000000000	16	48.58
	20		13	
	30		11	
	50		7	

Table VI shows the results of various test circuits (C17 bench mark circuit, 4-input, 6-input, 8-input, 10-input NAND gate circuits). For different population sizes (8, 20, 30, 50), MLVs are identified. Number iterations to locate MLV for various test circuits and their corresponding leakage powers are shown in the table for gravitational search algorithm.

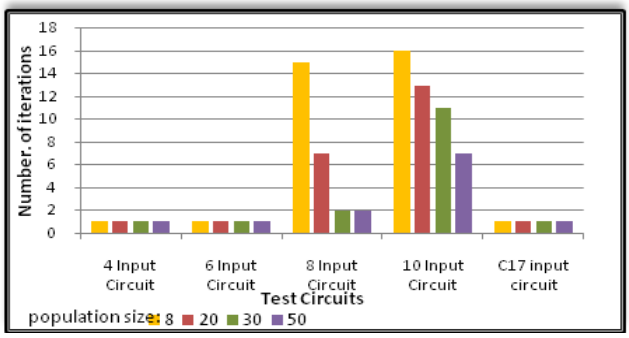

Fig. 22. Comparison of various bits of Test circuits of GSA

For different population sizes 8, 20, 30 and 50 of different bit sizes of NAND gate test circuits, a comparative analysis is carried out. Various test circuits vs. number of iterations to reach MLV are as shown in the above figure.

TABLE VII. Results obtained from various Algorithms

Test Circuit [10]	No. of Populat -ions	Number of Iterations		
		Genetic Algorithm	PSO Algorithm	Gravitational Search Algorithm
C17 circuit	8	1	1	1
4 input circuit	8	1	1	1
6 input circuit	8	15	5	1
8 input circuit	8	34	26	10
10 input circuit	8	96	62	13

Table VII and Fig. 23 show the number of iterations taken by GA, PSO and GSA to reach their global space. Here, comparison analysis is carried out with swarm size 8, to evaluate the algorithms, by using different test circuits.

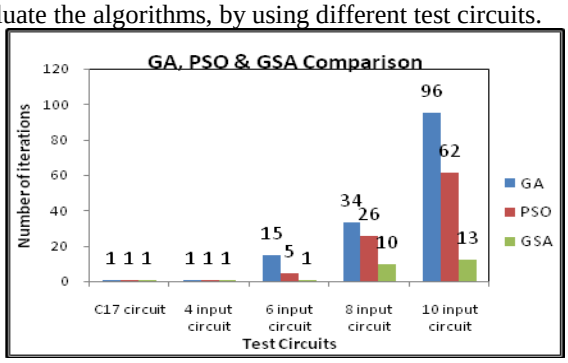

Fig. 23. Algorithms Comparison graph

C17 input test circuit MLV is identified as 00101for GSA, 10100 for PSO and 01000 for GA. However, according to the Table VI, at swarm size 8 for 10-input NAND gate test circuit, GA converges at 96 iterations, PSO converges at 62 iterations, whereas, GSA converges early in global space at 13 iterations as shown in the Fig. 24.

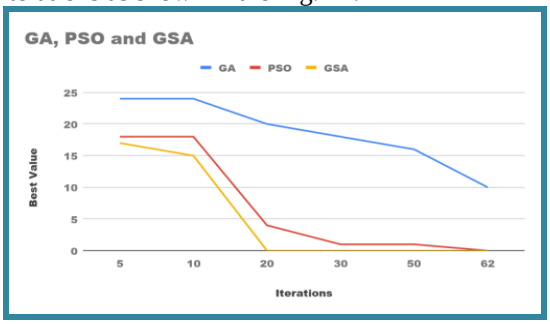

Fig. 24. Algorithm Convergence graph

In the comparative study (at population size 8) with other two algorithms: Genetic Algorithm and Particle Swarm Optimization Algorithm, GSA gives the better results as it consumes less leakage power and reaches its global space quickly. These results are shown in Table VII and Fig. 24.

The 16-bit input data is processed through the developed ALU circuit model and the simulation results are shown in Table VIII.

Table VIII. 16-bit Test Circuit MLP with GSA

Test Circuit	Input Vector in Binary Format	MLP with GSA (pW)	Maximum number of iterations
AND	A= 0110111001000110 B= 0110011100100110	20.13	16
OR	A= 0000000000000000 B= 0000000000000000	17.9	16
Adder	A= 0000000000000000 B= 0000000000000000	23.81	18
NAND	A= 0000000000000000 B= 0000000000000000	2.48	13
NOR	A= 0000000000000000 B= 0000000000000000	3.11	14
XOR	A= 1000000101001100 B= 0100111010000100	20.15	15
XNOR	A= 0101011010110010 B= 0111010011000001	21.89	15
NOT	A= 0000000000000000 B= 0000000000000000	4.45	10
SUB	A= 0000000000000000 B= 0000000000000000	25.52	17
INC	A= 0000000000000000 B= 0000000000000000	8.51	11

Table VIII represents the different input vector combinations of Test circuits with minimum leakage powers obtained with maximum number of iterations. For example, XOR test circuits with input vectors A, B considered in the above table achieved MLP with GSA is 20.15 pW attained in 15 iterations.

IX. CONCLUSION

A low power 16-bit ALU is designed with different Test circuits using PSPICE tool and leakage powers are obtained.

In this work, Gravitational search algorithm is used to locate the minimum leakage vector (MLV) and then, IVC technique is used to force all the other input vector combinations into minimum leakage state, so as to reduce leakage power. The main objective of leakage power reduction is carried out successfully by using IVC based GSA.Power analysis is done for 3-input test circuits to show the optimal power saving. Leakage power analysis is also carried out with AND test circuit with time varying graph. Finally, by using 4 input NAND gate, 6 input NAND gate, 8-input NAND gate, 10-input NAND gate and C17 bench mark circuits, a comparison study is done and it is proved that GSA gives better results in terms of minimum leakage power and number of iterations to converge into optimal solution, than GA and PSO.

GSA took 13 iterations to reach its global solution, whereas PSO took 62 iterations, and GA took 96 iterations.

X. FUTURE SCOPE AND LIMITATIONS

In this paper, 16-bit test circuits are constructed to form an ALU model so as to reduce the leakage power. Similarly, 32-bit and 64-bit test circuits can be constructed using the same PSPICE tool.

But the limitation to construct 32-bit or 64-bit ALU model is locating of MLV. For 16-bit test circuits, each test circuit has 65,536 (2^{16}) input combinations to find MLV. For 32-bit ALU model, for 4,29,49,67,296 input combinations – one has to verify to find MLV. It is a tedious process to locate MLV. Hence, random but judicial selection of input combinations is suggested to trace MLV, though it is not an exact solution.

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