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Low Voltage CMOS Power Amplifier with Integrated Capacitive Harmonic Termination

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Abstract: ***This paper presents a novel design methodology to improve the power added efficiency (PAE) for a CMOS power amplifier (PA), qualifying it for low voltage mobile wireless communications such as the NB-IoT. The capacitive harmonic termination (CHT) integrated at the output of the main stage PA to minimise the effect of the second harmonic distortion in order to improve the PAE. The CHT PA able to deliver a PAE of 40% at drain voltage of 3.3 V from 1.9 GHz - 2.1 GHz. The corresponding power gain is 14 dB for 200 MHz bandwidth. The achieved third-order intercept point (OIP3) is 33 dBm, which serves as a proof that the CHT technique has a minimal trade-off to the linearity performance of the PA.***

Keywords: Power Amplifier (PA), CMOS, Capacitive Harmonic Termination (CHT), Power Added Efficiency (PAE)

I. INTRODUCTION

The proliferation in the low voltage wireless communication system due to demand for high transmission data rate has imposed a great challenge in CMOS power amplifier (PA) design [1]. The distinct challenge is the trade-off between linearity and efficiency [2-4]. Various work has been proposed to improve the efficiency performance in CMOS PAs [5]. Among them are differential class-E PA, integrated phase linearizer class-AB PA, and resistive feedback class-D PA [6-9]. All this requires complex implementation and large chip size.

In this work, instead of the conventional short or open second harmonic termination which degrades the linearity performance of a PA, a CHT scheme is implemented to reduce the trade-off. CHT alters the drain voltage of the PA to be more than 2Vdd, therefore moving the non-linear region further away. This prevents early clipping of the drain voltage. Hence no effect on the linearity whilst PAE improves due to the cancellation implemented on the drain-source (CDS) capacitance.

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This paper is organized as follows. Section 2 explains the principle of operation of the CHT technique. In section 3, the corresponding results are presented and conclusion is given is section 4.

II. PRINCIPLE OF OPERATION

Figure 1 illustrates the operating concept of the CHT PA.

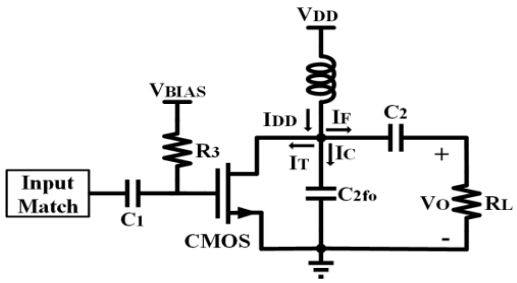
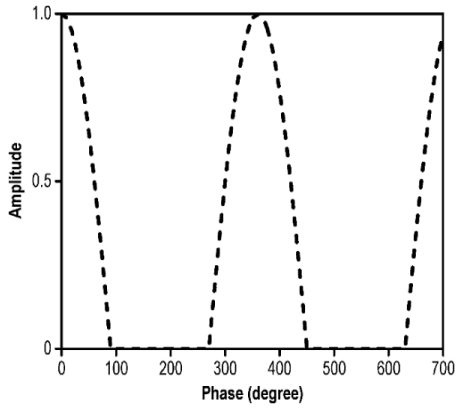
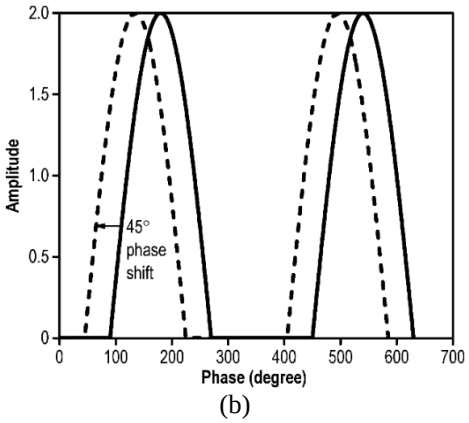


Fig. 1. The fundamental operation of CHT PA.

Its corresponding current and voltage waveforms are given in Figure 2.



(a)



(b)

Fig. 2. (a) Normalized current waveform and (b) Normalized voltage waveform of the CHT PA.

Due to the implementation of the CHT, the voltage waveform has been shifted 45º further away, thus reducing the overlapping to the current waveform. This greatly improves the efficiency. Since the voltage waveform's shape is not altered, the linearity performance of the PA is preserved. The corresponding output power is presented as:

$$P = v(\theta)I(\theta) \tag{1}$$

$$P = \pi V_{dc} I_{\max}(a).(b) \tag{2}$$

where,

$$a = \frac{1}{\pi} - \frac{1}{2}\cos(\theta+\phi) + \frac{2}{3\pi}\cos(2(\theta+\phi)) \tag{3}$$

$$b = \frac{1}{\pi} + \frac{1}{2}\cos\theta + \frac{2}{3\pi}\cos 2\theta \tag{4}$$

The corresponding impedance at second harmonic is given as:

$$Z_2 = j\left(\frac{3\pi}{8}\right)R_{load} \tag{5}$$

Figure 3 illustrates the implementation of the CHT PA in CMOS 180nm technology.

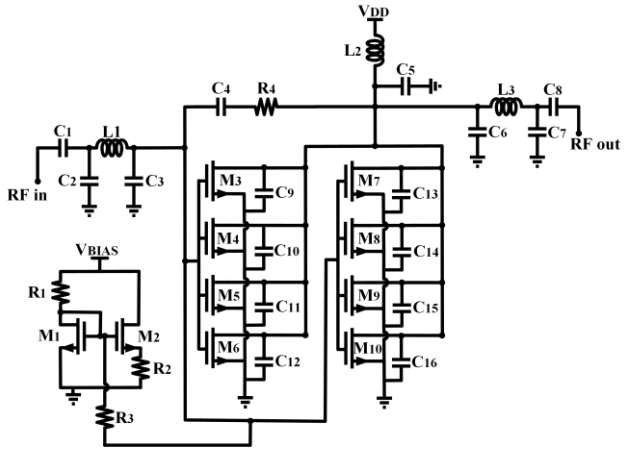


Fig. 3. Implementation of CHT PA.

It consists of 8 stages with individual termination to minimize the C_{ds} effect of each transistor. This is represented by C_9-C_{16}. The output matching network is represented by Pi-network consisting of C_6, L_3 and C_7. C_1 and C_8 serve as a DC block. A current mirror biasing circuit consisting of nMOS M_1 and M_2 is used to bias the PA in class-AB mode. To ensure stability and improve further the IMD3 performance which corresponds to OIP3, feedback network consists of R_4 and C_4 is utilized. This is illustrated from (6)-(8):

$$V_{out\_IMD3} = -\frac{1}{RC}\int V_{In\_IMD3}dt \tag{6}$$

$$V_{out\_IMD3} = -\frac{1}{RC}\int A_{IMD3}dt \tag{7}$$

where A_{IMD3} is the amplitude at the IMD3 frequency of $2\omega_2$-ω_1 and $2\omega_1$-ω_2. Hence,

$$V_{out\_IMD3} = -\frac{A_{IMD3}}{RC}(t) \tag{8}$$

The PAE is given as:

$$PAE(\%) = \frac{V_{out}I_{out} - V_{in}I_{in}}{V_{dd}I_{dd}} * 100\% \tag{9}$$

III. RESULT

Figure 4 illustrates the S-parameter performance of the CHT PA. It can be observed that it can deliver 14 dB gain from 1.90 GHz to 2.1 GHz with corresponding S11 and S22 less than -10 dB. A K-factor of more than 1 at aforementioned frequency indicates that the PA is unconditionally stable.

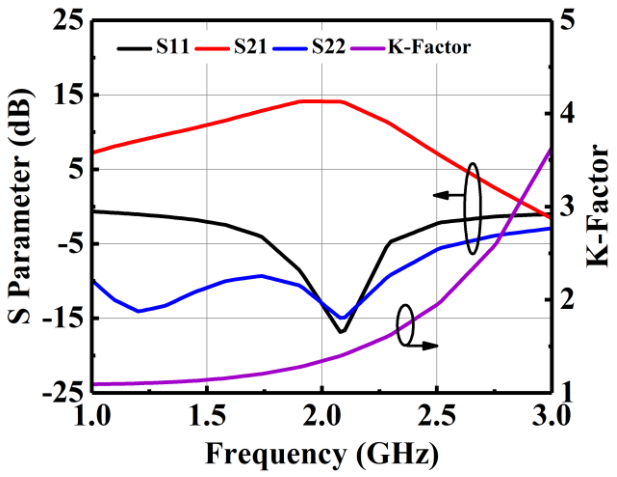


Fig. 4. S-parameter and stability (K-Factor)

performance of the CHT PA.

Figure 5 illustrates the larges signal gain and PAE from 1.9GHz to 2.1GHz of the CHT PA. Peak efficiency of 40% has been achieved across frequency with maximum output power of 24dBm. Large signal gain flatness of less than 1dB indicates that the PAE improvement is obtained via CHT technique does not impact the linearity performance of the PA. This can be further confirmed through the IMD3 (-33dBc) and OIP3 (33dBm) results obtained in Figure 6.

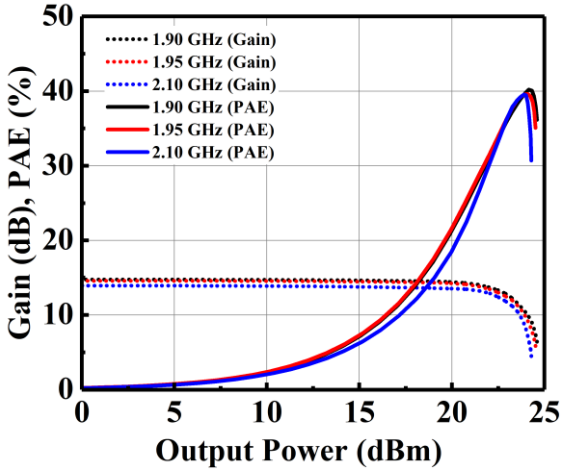


Fig. 5. Large signal gain and PAE performance of the CHT PA

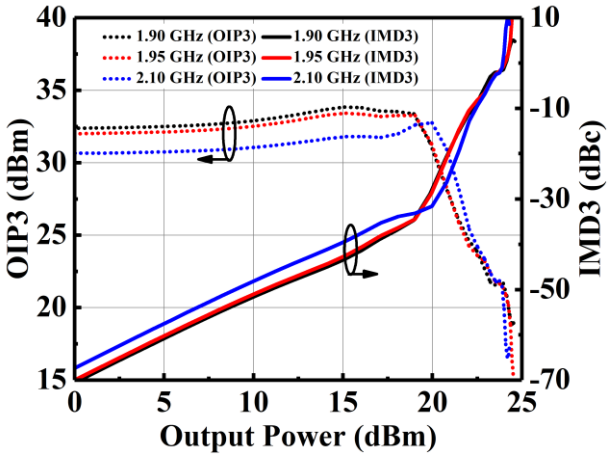


Fig. 6. Linearity performance of the CHT PA

Table I tabulates the performance summary while table II shows the performance summary and comparison with published work which clearly indicates the contribution of the CHT technique in improving the PAE of PA.

Table I. Performance summary

Parameter	Result		
Frequency (GHz)	1.90	1.95	2.10
Input return loss, S11 (dB)	-9.4	-12.1	-16.6
Gain, S21 (dB)	14.0	14.2	13.9
Output return loss, S22 (dB)	-10.8	-11.7	-14.9
Stability K-factor	1.2	1.3	1.3
Power gain (dB)	14.7	14.5	13.9
Output power (dBm)	24.5	24.5	24.3
PAE (%)	40.1	39.5	39.5
Linearity - OIP3 (dBm)	33.8	33.4	32.7
Supply voltage (V)	3.3		
CMOS Technology (nm)	180		

Table II. Performance summary and work comparison.

Reference	Freq. (GHz)	Max. Power (dBm)	Max. PAE (%)	Gain (dB)	Bandwidth (MHz)	Class
This work	1.9-2.1	24	40	14	200	J
[6]	2.4	22.8	31.1	18	Narrow	E
[7]	2.4-2.5	15	38.4	11.5	100	AB
[8]	0.6	16	36.6	20	Narrow	D
[9]	2.45	10	25.8	-	Narrow	D

IV. CONCLUSION

In this work, a novel efficiency improvement using CHT technique has been proposed which terminates the second harmonic distortion for the miniature PA. The fully integrated CHT PA is able to deliver more than 40% PAE with minimum trade-off to linearity for 200MHz of operating bandwidth. The ability to achieve the above mentioned performance at low output power qualifies the PA to be implemented in mobile phone transceivers such as NB-IoT.

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Sureshkumar Subramian received his B.Eng.Tech degree (Hons.) in Electrical from Universiti Teknikal Malaysia Melaka (UTeM) and currently pursuing M.Sc degree in Microelectronic System Engineering from Universiti Sains Malaysia (USM). His research interest includes CMOS RFIC mainly on PA for wireless communication system, Internet of things (IoT) and Internet of Everything (IoE) applications.

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Arvind Singh Rawat received his B.Tech degree in Instrumentation Engineering from USIC, HNB Garhwal University (Central Univeristy), Srinagar Garhwal, India, in 2009. He received his M.Tech (Hons) degree in VLSI Design from Faculty of Technology, Uttarakhand Technical University, India in 2013. From 2013, he is working as Assistant Professor in the Department of Electronics & Communication Engineering, Uttaranchal University, Dehradun. He His research interests include VLSI, Analog Integrated Circuit, Microelectronic.

Sofiyah Sal Hamid was born in Penang, Malaysia. She received her B. Eng. Degree with honors in Electronic Engineering in 2012, and MSc degree of Electronic Engineering in 2018 from Universiti Sains Malaysia (USM), Malaysia, respectively. In 2014, she joined Intel Microelectronic Malaysia as Analog RF Engineer. In 2015, she joined Collaborative Microelectronic Design Excellence Centre (CEDEC), USM as Research Officer in RF Analog IC Design. Her main research interest includes CMOS RF IC Design in Wireless and Mobile application