# Sleepy- Gate Diffusion Input (S-GDI) — Ultra Low Power Technique for Digital Design

**Anjali Sharma, Harsh Sohal**

*Abstract: In this paper we propose a power efficient technique called Sleepy- Gate Diffusion Input (S-GDI) that can be used for efficient digital design at nano scale foundries. For area and power comparison, ten prior techniques are taken in to consideration and applied on XOR gate, 1-bit adder, 1-bit comparator and 4- bit up-down counter. All techniques are parametrically analyzed on 65nm technology. The proposed S-GDI technique has been observed power efficient as compared to Complementary CMOS technique (CCT), Complementary Pass Transistor Logic (CPTL), DCMOS (Differential CMOS), Differential Cascode Voltage Switch with Pass Gate Logic (DCVSPG), Energy Economized Pass Transistor Logic (EEPL), Lean Integration with Pass Transistors (LEAP), Push-Pull Pass Transistor Logic (PPL), Pass Transistor Logic (PTL), CMOS with Transmission Gate (TG) and Gate diffusion Input (GDI). As compared to GDI technique S-GDI is showing 96.20%, 93.65%, 97.88% and 98.22% power efficiency for XOR, 1-bit adder, 1-bit comparator and 4-bit up-down counter respectively. S-GDI is showing area efficiency of 17.16% and 28.1% for XOR, 41.26% and 53.89% for 1-bit adder, 7.6% and 21.76% for 1-bit comparator and 6.7% and 28% for up-down counter over EEPL and DCMOS technique respectively. Although other techniques except EEPL and DCMOS techniques are area efficient as compared to proposed technique but this is on the expense of higher total power dissipation. So, PDP (power delay products) of all considered techniques are also calculated on 65nm technology for both SUM and CARRY outputs of 1-bit adder. In both cases power delay product for S-GDI technique is very less as compared to all other considered technique. Due to efficiency of S-GDI in terms of considered parameters, this technique can be efficiently used for low power applications.*

*Keywords: CMOS, Gate diffusion Input (GDI), MTCMOS, nm, sleep transistor (ST), Sleepy- Gate Diffusion Input (S-GDI), VLSI.*

## I. INTRODUCTION

Increasing demand of power efficient portable and implantable electronics on VLSI chips is leading to contemporary advancement in ultra-low power designs. VLSI design techniques are required with higher power efficiency and throughput. Dissipated heat must be removed effectively to keep temperature of implantable electronics in acceptable level [1]. For designing any ultra-low power circuit it is necessary to take all power estimation and optimization factors into consideration. Therefore, in order to decrease the dissipation up to admissible level, optimized ultra-low power designing techniques are required [2]. Static and dynamic power dissipation together constitutes total power dissipation in any VLSI circuit. Leakage current is one of the dominant factors for static power dissipation in nano scale VLSI design which depends on leakage below threshold, leakage at reversed biased PN junction and leakage due to carrier tunneling [3]. Dynamic power dissipation depends on activity factor, load capacitance, switching frequency and supply voltage. Small sized transistors with minimum channel width when operated at lower supply voltage cause increase in static power dissipation [4]. Low power design methodology can be optimized at different abstraction level. At system level partitioning and power gating can be done for optimization whereas at algorithm level complexity, concurrency and regularity can be checked. Optimization may be done at planning level, logic level and technology level. At logic level logic style changes and transistor resizing can be performed. Threshold reduction and multithreshold devices can be used at technology level [5].

This paper focuses on technology and logic level optimization and proposes a new improved low power technique named as "S-GDI (Sleepy- Gate Diffusion Input)". Although S-GDI technique comes with an area overhead as compared to GDI, but at the same time it is showing extremely high power efficiency. The main additions of this paper are: 1) Designing structure of S-GDI 2) S-GDI 1-bit comparator operation 3) Comparative analysis of S-GDI technique with other considered techniques.

## II. PREVIOUS CONTRIBUTION

Prior contribution in the field of power reduction techniques are briefly discussed in this segment. Complementary MOS technique (CMOS) is one of the basic techniques used for digital circuit designing. Circuit implementation by Pass Transistor Logics (PTL) has shown enhanced performance as compared to CMOS technique in terms of speed, area and power efficiency. Algebraic factorization can be used for further optimization of PTL based circuits [6-8]. Circuit families can be compared in terms of area, static power dissipation, their robustness and their ability of efficient cascading with other circuits on the same chip [4]. Algorithm level power optimization can be done by making decision diagram in terms of binary numbers [9]. Changes in boolean diagrams can be done to achieve circuit efficiency.

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These boolean diagrams can be mapped, one to one in PTL cell. Mapping of boolean representation to PTL logic by reversing their order can achieve efficiency in terms of dynamic power dissipation due to less switching activities [10]. Power dissipation can be reduced in pass transistor technique by replacing NMOS with PMOS [11-12]. An alternative design methodology for low power circuit designing is Dual Model Logic (DML) family. DML gate can be used for switching between static and dynamic mode of circuit operation as per the requirement. Energy efficiency with moderate performance can be achieved in static mode, whereas performance efficiency can be achieved by losing energy efficiency in dynamic mode [13]. Differential Cascode Voltage Switch Logic (DCVSL) and Complementary Pass Transistor Logic (CPTL) are other circuit designing techniques with some different circuit structure and higher delay. Delay of circuit designed by these techniques can be lowered by other technique called DCVSL-R where R stands for resistor. DCVSL-R provides lower delay on the expense of increased parasitic effects and area. These parasitic effects can be decreased by replacing R with Ultra-Low-Power Diode (ULPD) structures [14]. Use of multithreshold transistor is one of the technology level optimization in which transistors with different thresholds are used for circuit designing. Low-threshold voltage MOSFET are speedy but having larger leakage current whereas high-threshold voltage MOSFET are having opposite parameters as compared to low threshold transistors [15]. Standby switching can be employed for turning off high threshold voltage transistors in sleep mode, which can also decrease the leakage current trough the circuit [16]. Static power dissipation increases at low nm technologies where maintaining the appropriate size of the transistor is one of the major challenge. There are various ways of maintaining proper transistor size in MTCMOS circuits [17]. Use of sleep transistor with an actual logic implementation can reduce static power dissipation in digital circuits [18]. Although sleep transistor reduces the power dissipation but its optimization at logic level is quite difficult on nano meter foundries [19-20]. Hybridized double pass transistor technique with MTCMOS has reduced the area consumption as well as subthreshold leakage which are one of the reasons for static power dissipation [21].

Hybridization of various concepts of power reduction can be helpful in introducing a new low power technique for low nm technologies [22-25]. Full output voltage swing and less noise is required for efficient implementation of any digital circuit. GDI (Gate-Diffusion-Input) is another technique in the literature which can provide power and speed efficiency along with full voltage swing at the output [26-30]. Efficiency of GDI technique can be improved by using Mixed Threshold Voltage (MVT) scheme [31]. Circuit structures with different applied clocks can also help in achieving power and speed efficiency [32-33]. Transistor gating techniques can also be used for power reduction but it suffers from poor reliability due to ground bounce problem which can further be overcome by sleep transistor [34]. FinFETs can be the replacement of MOSFETs when power efficiency is required at nano meter technologies. FinFETs can be used with the concept of power gating and sleep transistor to reduce the power dissipation. Individual optimization of NMOS and PMOS can also be helpful in obtaining power efficiency. Also, upgraded and advanced fabrication technologies as compared to CMOS technology can be used to achieve power and speed efficiency [35-37].

Comparative analysis of the proposed "S-GDI (Sleepy-Gate Diffusion Input)" technique is done with ten prior techniques which are Complementary CMOS technique (CCT), Complementary Pass Transistor Logic (CPTL), DCMOS (Differential CMOS), Differential Cascode Voltage Switch with Pass Gate Logic (DCVSPG), Energy Economized Pass Transistor Logic (EEPL), Lean Integration with Pass Transistors (LEAP), Push-Pull Pass Transistor Logic (PPL), Pass Transistor Logic (PTL), CMOS with Transmission Gate (TG) and Gate diffusion Input (GDI). Considered parameters for comparison are delay, area and power. Same ratios of length and width are maintained for MOS devices i.e. 6 for PMOS and 3 for NMOS. Concept of MTCMOS is also used in proposed technique.

## III. S-GDI STRUCTURE

S-GDI technique has a structure of the GDI with sleep transistor. For actual logic implementation GDI modules have been used because of its area and power efficiency. Sleep transistor is used with those MOS in the GDI module which is having direct connection with $V_{DD}$ and $V_{SS}$. S-GDI can achieve ultra-low power dissipation as compared to all considered previous approaches. We first explain the circuit structure of four basic functions by S-GDI modules and then S-GDI 1-bit comparator is taken as an instance for explaining the working of S-GDI technique in operational mode. Circuit structures of S-GDI modules for four different operations are shown in Figure 1 and 2.

These digital functions by S-GDI technique is different from basic GDI technique [38-39] because it uses sleep transistors and can give its operation in active and inactive (sleep) mode. Sleep transistors with greater threshold value are used between $V_{DD}$ & MOS transistor and $V_{SS}$ & MOS transistor which make an isolation of GDI logic structure from $V_{DD}$ and $V_{SS}$. Because of the use of sleep transistors, this modified structure saves the power in inactive (sleep) mode as well as in active mode. Use of high threshold transistor in the circuit helps in lowering the static power dissipation. Actual logic expression is implemented by low threshold MOS devices. W/L=6 and 3 is maintained for all PMOS and NMOS transistors respectively. High threshold PMOS transistor is used between $V_{DD}$ and one of the terminals of the transistor involved in the logic design and NMOS transistor with higher threshold voltage is used between $V_{SS}$ and one of the terminals of the transistor used for logic implementation. For circuit operation in active mode SLEEP input is kept "1" because for NMOS sleep transistor to act as closed switch input should be high. Whereas SLEEP BAR input is kept low because for PMOS sleep transistor to act as closed switch input should be low. In sleep mode SLEEP is kept low and SLEEP BAR is kept high. Operation of S-GDI modules for active mode AB=11 is shown in Figure 2. Red input box and output LED is showing high logic whereas non glowing input box is showing low logic. Operation table for S-GDI functions in active mode are shown in Table I.
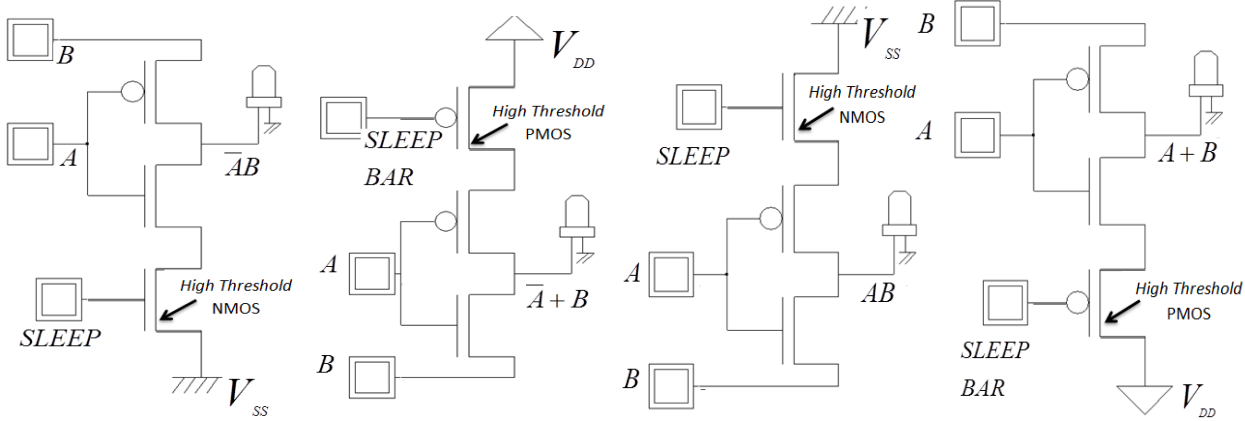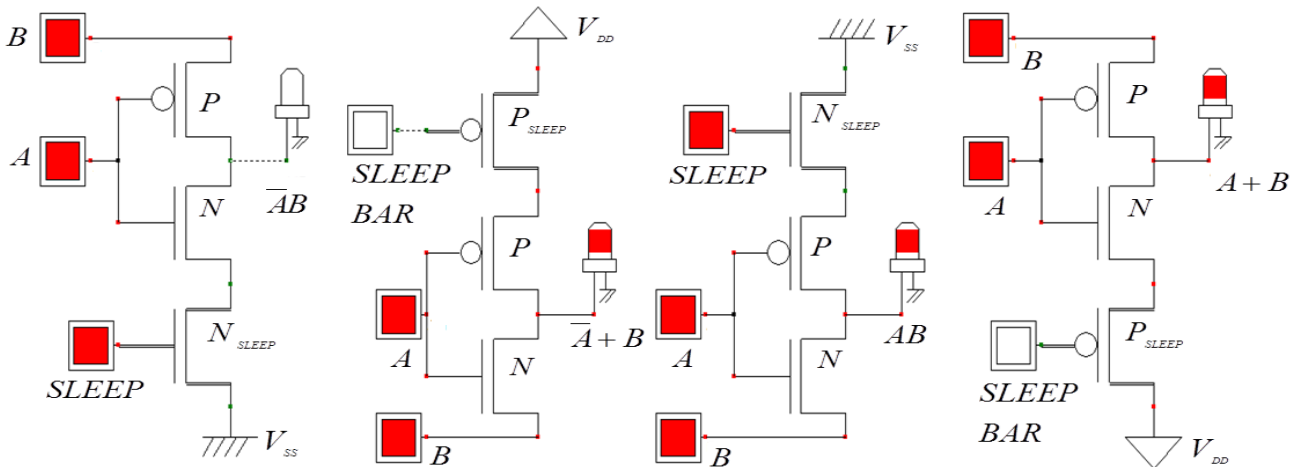
**Fig. 1. Digital functions by S-GDI technique.**



**Fig. 2. S-GDI digital functions in active mode**

**Table- I: Operation Table for Various Logic Functions by S-GDI in Active Mode**

| SLEEP | SLEEP BAR | $S_{P_{SLEEP}}$ | $S_{N_{SLEEP}}$ | $S_P$ | $G_{P,N}$ | $S_N$ | $OUT_{D_{P,S}}$ | WHERE | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | — | — | — | $V_{SS}$ | $B$ | $A$ | $D_{N_{SLEEP}}$ | $\overline{AB}$ | $S_{P_{SLEEP}}$ | Source of PMOS sleep Transistor | $D_{P_{SLEEP}}$ | Drain of PMOS sleep Transistor |
| — | O | $V_{DD}$ | — | $D_{P_{SLEEP}}$ | $A$ | $B$ | $\overline{A}+B$ | $S_{N_{SLEEP}}$ | Source of NMOS sleep Transistor | $D_{N_{SLEEP}}$ | Drain of PMOS sleep Transistor |
| 1 | — | $V_{DD}$ | $V_{SS}$ | $D_{N_{SLEEP}}$ | $A$ | $B$ | $A+B$ | $S_P$ | Source of PMOS Transistor used for logic implementation | $OUT_{D_{P,S}}$ | Output at drain of NMOS and PMOS transistor used for logic implementation |
| — | O | — | — | $B$ | $A$ | $D_{P_{SLEEP}}$ | $AB$ | $G_{P,N}$ | Gate of PMOS and NMOS used for logic implementation | $S_N$ | Source of NMOS Transistor used for logic implementation |

## A. Operational analysis of S-GDI circuits

Circuit design of 1-bit S-GDI comparator on 65nm CMOS technology is shown in Figure 3 which is showing its operation during active modes. Sleep transistors are having threshold voltage twice as taken for transistors used for logic implementation. Width of sleep transistors is taken such that it maintains the W/L ratio of (W/L=3) for all NMOS and W/L ratio of (W/L=6) for all PMOS. Circuits designed by S-GDI technique do its functionality when all sleep transistors work in active mode.

In inactive (sleep) mode, sleep transistors act as an open switch which makes the isolation of low threshold transistors from $V_{DD}$ & $V_{SS}$ hence decreasing the leakage current. In active mode operation of 1-bit comparator, SLEEP input=1 and SLEEP BAR input=0. Due to the use of this input combinations, sleep transistors act as a close switch and give a close path from $V_{DD}$ & $V_{SS}$. Because of this continuous path, delay in the circuit can be reduced. SLEEP (inactive) mode operation of 1-bit comparator can be achieved when SLEEP input=0 and SLEEP BAR input=1. Due to the use of this input combinations, sleep transistors go in off mode and disconnect the connection of circuit with $V_{DD}$ & $V_{SS}$. Power efficient digital designs can be done by proposed S-GDI technique but this can account area inefficiency as compared to GDI.
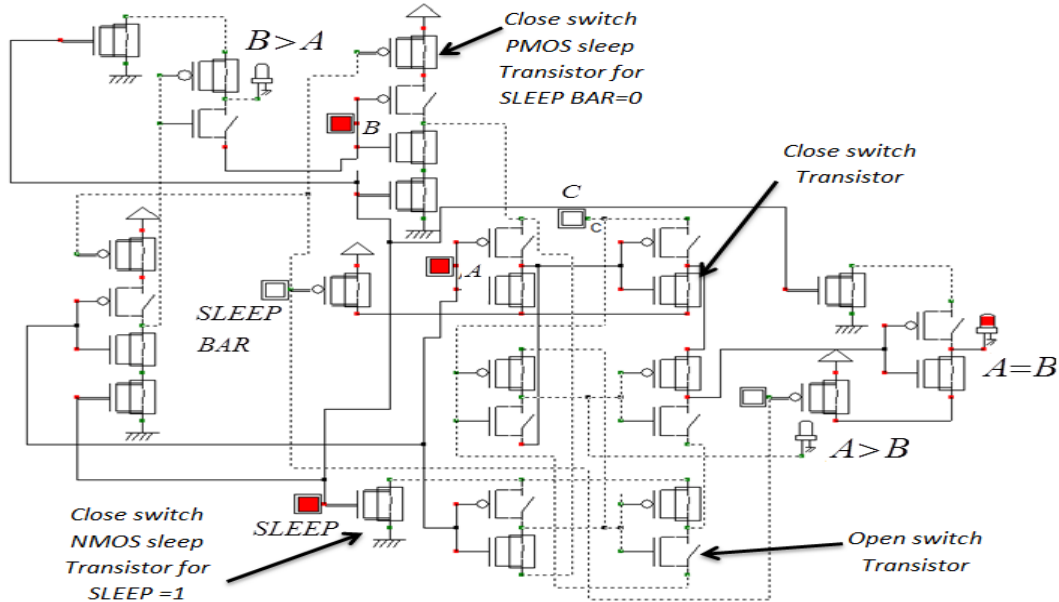


**Fig. 3. S-GDI 1-bit comparator in active mode**

## IV. DIGITAL CIRCUITS BY S-GDI TECHNIQUES

This segment targets on four benchmark circuits on which various techniques are applied on 65nm CMOS technology. These benchmark circuits are designed by ten different techniques while maintain the same width and lengths values for all MOS transistors.

### A. Operational analysis of S-GDI circuits

To analyze the S-GDI technique on general logic design four basic digital circuits are considered: XOR Gate, 1-bit full adder, 1-bit comparator and 4-bit up-down counter. All circuits by S-GDI technique and their operational waveforms are shown in Figure 4 (a-h). XOR gate uses 3 NMOS and 3 PMOS transistors, 1-bit full adder uses 7 NMOS and 7 PMOS, 1-bit comparator uses 15 NMOS and 14 PMOS and 4-bit up-down counter uses 62 NMOS and 54 PMOS transistors for circuit design by S-GDI technique. Timing diagram of these circuits have shown correct logic implementation of these circuits by S-GDI technique. In sleep mode of timing diagrams no operation is performed by the circuits. In active mode actual operation of all circuits can be analyzed from the timing diagram.
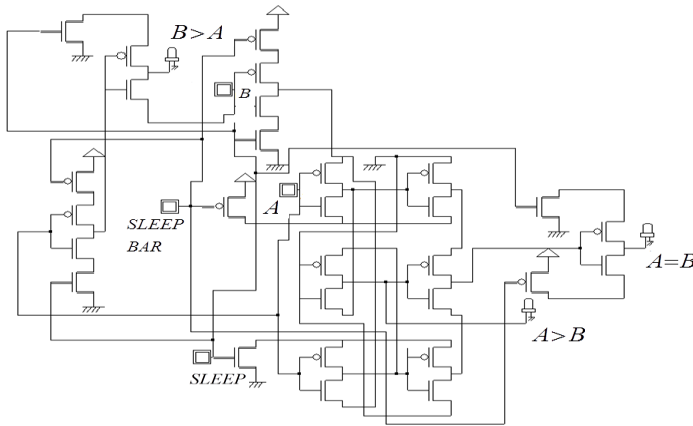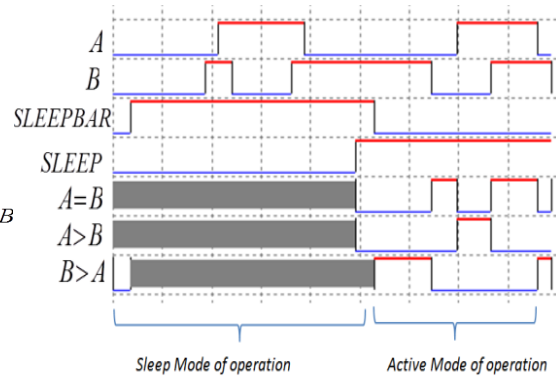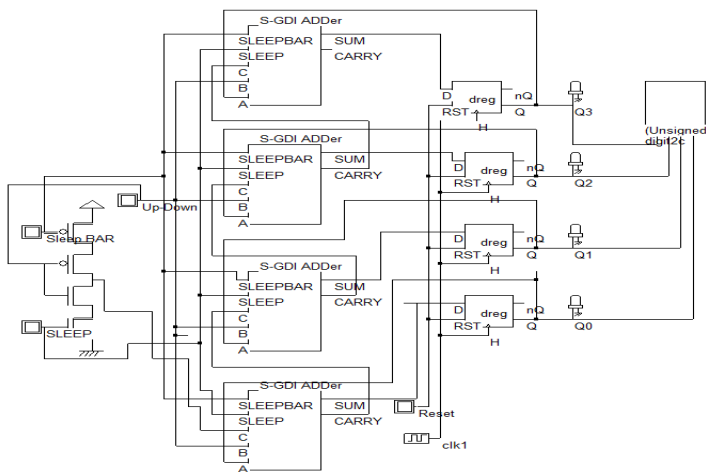


a) S-GDI XOR gate



b) Timing diagram of S-GDI XOR gate
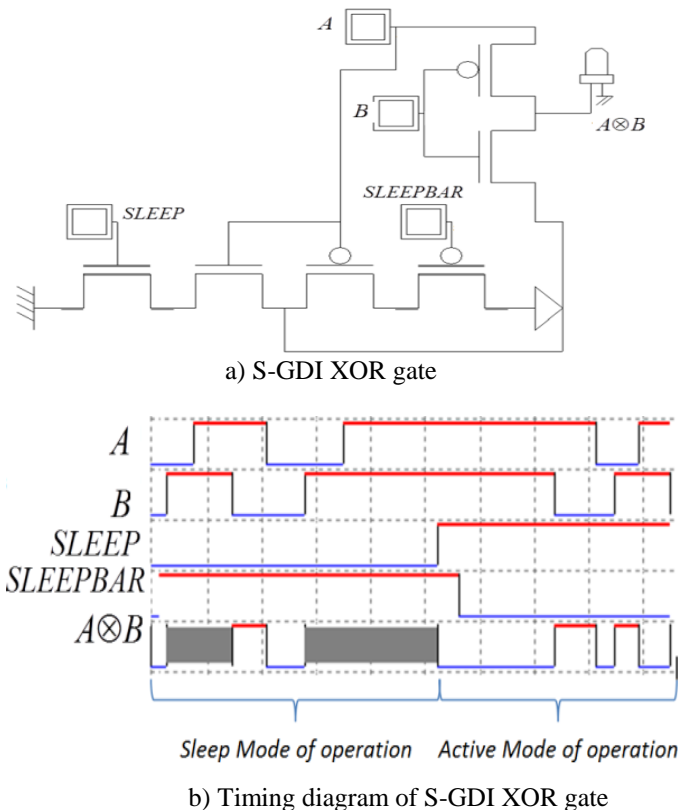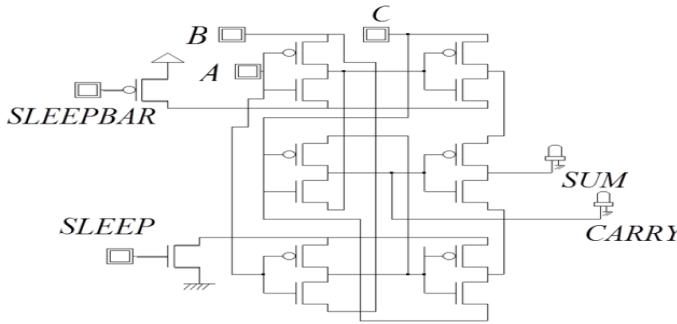
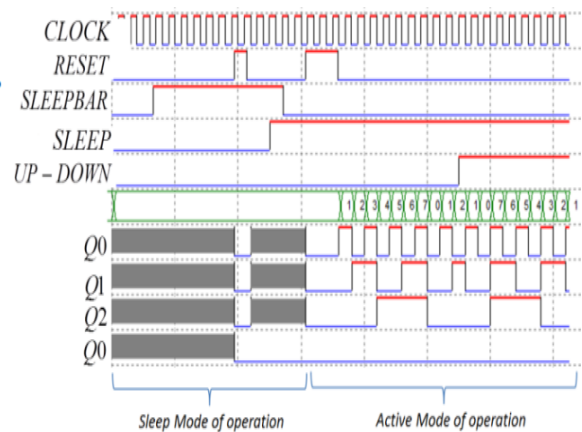**c) S-GDI 1-bit full adder**
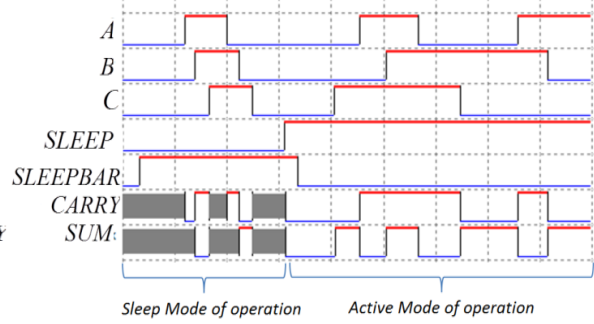


**d) Timing diagram of S-GDI 1-bit full adder**



**e) S-GDI 1-bit comparator**



**f) Timing diagrams of S-GDI 1-bit comparator**



**g) S-GDI 4-bit up-down counter**



**h) Timing diagrams of S-GDI 4-bit up-down counter**

**Fig. 4.a-h) Benchmark circuits by S-GDI**

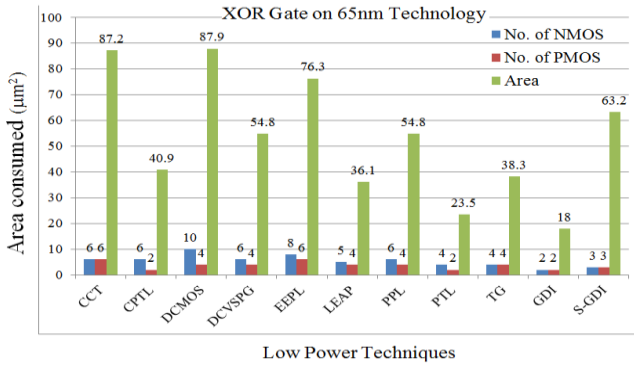## V. COMPARISON WITH OTHER DESIGN TECHNIQUES

This segment presents simulation results for digital circuits using BSIM-4 model on 65nm CMOS technology on $27^0$C. Schematic designs and their waveforms for these circuits designed by S-GDI are already presented in segment 4. Schematics of these circuits by all considered techniques are designed on DSCH 3.8. Simulation timing waveforms are analyzed to observe proper functioning of these circuits. An error free layout is these circuits are generated by compiling verilog files on Microwind 3.8.1 beta. These layouts are further parametric analyzed to achieve total power dissipation and delay. Parametric analyses in terms of total power dissipation are done for 0.5V, 0.7V and 0.9V input voltages.

Some compromises of proposed technique is observed in terms area consumption but at the same time this techniques is showing its power efficiency as compared to all other considered techniques.

### A. Analysis for area consumed

Figure 5 presents the area occupied by digital circuits designed by all considered techniques on 65nm CMOS technology. Figures display the required no. of NMOS and PMOS transistors and their corresponding area consumed for designing benchmark circuits by different low power techniques. S-GDI is showing area efficiency of 17.16% and 28.1% for XOR, 41.26% and 53.89% for 1-bit adder, 7.6% and 21.76% for 1-bit comparator and 6.7% and 28% for up-down counter over EEPL and DCMOS technique respectively.

*Retrieval Number: A4998119119/2019©BEIESP*
*DOI: 10.35940/ijitee.A4998.119119*
*Journal Website: www.ijitee.org*

*Published By:*
*Blue Eyes Intelligence Engineering*
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**a) Area consumed by XOR gate**
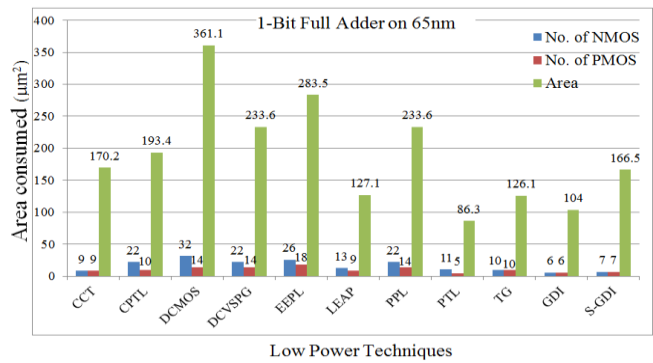


**b) Area consumed by 1-bit full adder**



**c) Area consumed by 1-bit comparator**



**d) Area consumed by 4-bit up-down counter**

**Fig. 5.a-d) Area consumed by the digital circuits on 65nm CMOS technology**

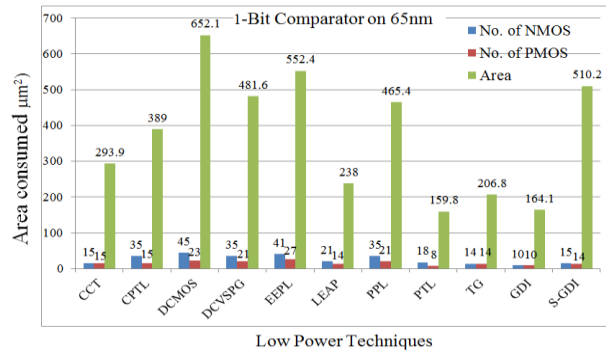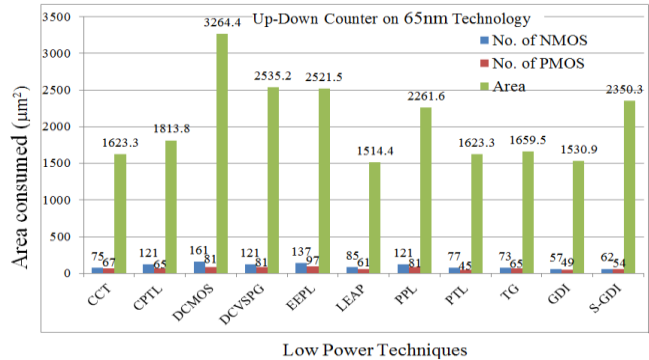## B. Analysis for power dissipation

Observations of total power dissipated by all designed circuits are carried out on three input voltage supplies i.e. 0.5V, 0.7V and 0.9V. Although the area consumed by some of the considered techniques are less as compared to the area consumed by the S-GDI designs but this on the expense of higher power dissipation. Total power dissipated by different techniques for considered digital circuits are shown in Table-II which presents that total power dissipation increases with the increase in supply voltage. Proposed S-GDI technique proves to be more power efficient as compared to all considered techniques on 65nm technology. As compared to GDI technique S-GDI is showing 96.20%, 93.65%, 97.88% and 98.22% power efficiency for XOR, 1-Bit Adder, 1-bit comparator and 4-bit up-down counter respectively.

**Table-II: Total Power Dissipation by the Benchmark Circuits on 65nm Technology**

| Low Power Techniques | Total Power Dissipation by the Benchmark Circuits on 65nm Technology (µW) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | XOR Gate | | | 1-bit adder | | | 1-bit comparator | | | 4-bit up-down counter | | |
| | 0.5 V | 0.7V | 0.9V | 0.5 V | 0.7V | 0.9V | 0.5 V | 0.7V | 0.9V | 0.5 V | 0.7V | 0.9V |
| CCT | 1.249 | 2.497 | 4.203 | 1.938 | 3.92 | 6.775 | 3.977 | 12.16 | 25.996 | 10.891 | 27.663 | 53.736 |
| CPTL | 0.557 | 1.118 | 1.896 | 2.592 | 8.363 | 25.368 | 5.666 | 17.87 | 47.994 | 9.278 | 26.355 | 76.678 |
| DCMOS | 5.826 | 17.06 | 41.34 | 16.092 | 53.68 | 77.803 | 16.289 | 47.13 | 94.873 | 40.627 | 133 | 269 |
| DCVSPG | 0.953 | 1.909 | 3.242 | 2.809 | 8.713 | 24.596 | 5.852 | 17.86 | 45.032 | 8.418 | 23.26 | 62.879 |
| EEPL | 1.33 | 2.718 | 4.787 | 5.081 | 13.27 | 33.071 | 8.710 | 30.30 | 69.653 | 11.102 | 35.806 | 88.636 |
| LEAP | 2.541 | 7.278 | 14.37 | 1.978 | 7.402 | 20.545 | 4.174 | 17.28 | 45.035 | 4.607 | 47.029 | 105 |
| PPL | 0.981 | 3.231 | 12.50 | 3.369 | 11.79 | 37.904 | 6.733 | 23.27 | 62.892 | 7.588 | 21.964 | 59.150 |
| PTL | 0.369 | 0.734 | 1.242 | 0.927 | 3.063 | 9.973 | 1.738 | 4.393 | 10.493 | 2.158 | 15.56 | 44.234 |
| TG | 0.716 | 1.432 | 2.416 | 2.118 | 4.194 | 7.067 | 3.535 | 7.287 | 12.471 | 4.495 | 9.840 | 19.247 |
| GDI | 0.172 | 0.343 | 0.599 | 0.065 | 0.205 | 0.435 | 1.148 | 2.464 | 4.613 | 2.704 | 6.562 | 17.45 |
| S-GDI | 0.007 | 0.013 | 0.022 | 0.007 | 0.013 | 0.022 | 0.027 | 0.052 | 0.086 | 0.095 | 0.187 | 0.309 |

## C. Analysis for delay

For the illustration of delay comparison 1-bit full adder design has been analyzed on 65nm CMOS technology. On this foundry 0.07µm is taken as a channel length for all MOS devices whereas widths are taken such that they maintain W/L equal to 6 and 3 for all PMOS's and NMOS's respectively. Individual delay at SUM and CARRY output has been analyzed for each technique.

Rise time, fall time and average propagation delay for SUM and CARARY outputs of 1-bit full adder is shown in Table III.

**Table-III: Rise time, fall time and average propagation delay for 1-bit full adder**

| Power Reduction Techniques | 1-bit full adder on 65nm | | | | | |
|---|---|---|---|---|---|---|
| | Delay at SUM output | | | Delay at CARRY output | | |
| | Rise Time (ps) | Fall Time (ps) | Average Delay (ps) | Rise Time (ps) | Fall Time (ps) | Average Delay (ps) |
| CCT | 157 | 288 | 222.5 | 105 | 10 | 57.5 |
| CPTL | 119 | 1048 | 583.5 | 1098 | 6 | 552 |
| DCVSPG | 181 | 1051 | 616 | 1120 | 7 | 563.5 |
| EEPL | 213 | 1158 | 685.5 | 1046 | 75 | 560.5 |
| LEAP | 2136 | 31 | 1083.5 | 2136 | 31 | 1083.5 |
| PPL | 182 | 1062 | 622 | 1132 | 5 | 568.5 |
| PTL | 101 | 14 | 57.5 | 2074 | 5 | 1039.5 |
| TG | 19 | 137 | 78 | 10 | 10 | 10 |
| GDI | 746 | 634 | 690 | 32 | 59 | 45.5 |
| S-GDI | 272 | 39 | 155.5 | 27 | 149 | 88 |

From Table III it can be inferred that proposed S-GDI technique is having less average propagation delay as compared to CCT, CPTL, DCVSP, EEPL, LEAP, PPT and GDI at SUM output. At carry output proposed S-GDI technique is having less average propagation delay as compared to CPTL, DCVSP, EEPL, LEAP, PPT and PTL technique. Delay of S-GDI technique is 30.11%, 73.35%, 74.75%, 77.31%, 85.64%, 75% and 77.46% less as compared to CCT, CPTL, DCVSP, EEPL, LEAP, PPT and GDI at SUM output respectively. At the same time delay of S-GDI technique is 84.05%, 84.38%, 84.29%, 91.87%, 84.52% and 91.53% less as compared to CPTL, DCVSP, EEPL, LEAP, PPT and PTL at CARRY output respectively. Although TG and GDI are efficient in terms of delay as compared to S-GDI technique but at the same time these techniques are giving power inefficiency as compared to S-GDI.
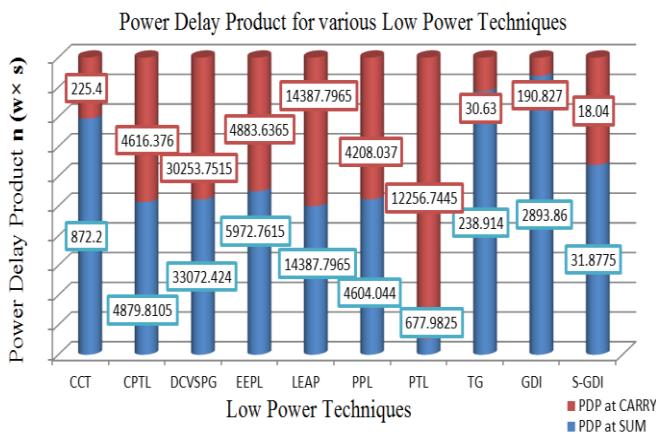


**Fig. 6. PDP of different techniques for 1-bit full adder circuit**

Figure 6 displays the PDP (power-delay products) of various techniques, which are calculated to account further verification of S-GDI technique for both SUM and CARRY output on 0.7V input supply voltage. Efficiency of S-GDI as compared to all other techniques in terms of PDP can be further recognized from the Figure on 65nm technology.

## VI. CONCLUSION

In this paper, we proposed a power efficient technique for leakage dominant CMOS foundries called S-GDI (Sleepy-Gate diffusion Input). In circuit structure of S-GDI technique, high threshold sleep transistors are used with the concept of GDI. Theses high threshold sleep transistors are used with those MOS in the GDI module which is having direct connection with $V_{DD}$ and $V_{SS}$. To demonstrate the implementation of S-GDI technique on digital modules, we have designed XOR Gate, 1-bit full adder, 1-bit comparator and 4-bit up-down counter on Microwind 3.8 beta. Same digital circuits are designed by ten previous techniques and compared on 65nm CMOS technology in terms of three parameters i.e. area consumption, total power dissipation and delay. S-GDI technique is power efficient as well as efficient in terms of PDP as compared to all other considered techniques. Parametric analyses for 1-Bit adder in terms of PDP and delay are carried out for SUM and CARRY output. All circuits are parametrically analyzed on BSIM-4 MOS model. From parametrical analysis S-GDI is proved efficient for digital circuit design at nm CMOS technologies as compared to all other considered techniques. In applications like implantable electronics where less power dissipation is of utmost importance, proposed technique can be efficiently used for circuit designing.

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*Retrieval Number: A4998119119/2019©BEIESP*
*DOI: 10.35940/ijitee.A4998.119119*
*Journal Website: www.ijitee.org*

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