Energy Efficient SRAM

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Abstract: Memories are an essential unit of any digital circuit, thus their power consumption must be considered during the designing process of the cells. To improve performance, reduce delay and increase stability, it is advisable to decrease the power consumed by the memory. Due to high demand of speed, high performance, there's a need to decrease the size of the device, thereby increasing the devices placed per chip. This high integration makes chips more complex but improves device performance. Design of SRAM cells with speed and low power is crucial so as to replace DRAMs. The layout of SRAM has advanced to meet the requirements of the present industry in accordance with parameters like delay, power consumption and stability etc. This paper presents the aim of analyzing different technologies used to make SRAM more efficient in terms of parameters such as static noise margin, latency and dissipation of power. The stability investigation of SRAM cells are usually derived from the Static Noise Margin (SNM) analysis. Here we observe a SRAM design which has used dynamic logic and pass transistor logic. We further study the effects made on this design by employing various technologies such as AVL-S, AVL-G, AVL and MT-CMOS, at 180nm CMOS technology to achieve enhancements in delay, power consumption and performance. The proposed circuits are simulated and the results obtained have been analyzed to show significant improvement over conventional SRAM designs. Cadence Virtuoso simulation is used to confirm all the results obtained in this paper for the simulation of 180 nm CMOS technology SRAMs.

Index Terms: Static Random Access Memory, Static Noise Margin, Adaptive Voltage Level Technique, Multi-Threshold CMOS.

I. INTRODUCTION

In any device, memories serve as an important segment and help in storage and retrieval of data. When it comes to the space they occupy, they cover more than 50% of the area of any device in today's world. Memory devices are simple circuits which store information in the binary format in large quantities. The demand for high capacity, performance and speed has led to the reduction in the size of the device, to accommodate some devices that can be placed on the single system on chip (SoC).

Memories may be further classified as Random Access Memory (RAM) and Read Only Memory (ROM). RAM stores information required during the execution period and is volatile, that is, when the power is tuned off, the bits stored are lost; whereas Read Only Memory is the memory which retains the data even after power loss. RAM is divided into Static RAM (SRAM) and Dynamic RAM (DRAM). One of the key differences between SRAM and DRAM is that Dynamic RAM has to be periodically refreshed whereas the Static RAM retains the data or information provided that the power is supplied to the cell. SRAM is intended to fulfill two needs. One is to furnish an immediate interface with the computer hardware at rates not achievable by DRAM, and the other is to supplant DRAM in frameworks that require low power utilization. SRAM is the real supporter of the power dissemination, as they involve a noteworthy segment of Systems-on-Chip (SoCs), and their bit will increase more later on.

II. LITERATURE SURVEY

The paper by Rosalind Deena Kumari Selvam et al proposed a SRAM cell design to lower power dissipation and increase speed, i.e., decrease delay. This is done by employing pass-transistor logic and dynamic logic. The dynamic logic is used to uphold the voltage degradation by employing NMOS and PMOS transistors, similar to the CMOS logic, even though NMOS transistors are used in the cell majorly. Significant improvement in power dissipation is seen in the proposed circuit by 99.64%, latency by 99.9% and 490Mbps of throughput.

This proposed technique reduced the amount of transistors used as compared to other CMOS techniques. This is made possible because the pass transistor logic is used by the function transistors to pre charge those transistors (PMOS and NMOS) which are employed in the working of a logic function.

Better performance is noticed in this proposed 8T SRAM cell. This model was analyzed using domino logic at 70, 90, 120 and 180 nm. Improvements in various parameters such as power dissipation, delay, throughput, efficiency etc were seen as a result of the analysis.

Using this as the basis of our research, we have applied various power reduction techniques to make a more efficient SRAM. These techniques and consequent results obtained are described in this paper.

III. LEAKAGE REDUCTION TECHNIQUES

A. Conventional 6T SRAM Cell

A 6 Transistor cell includes 2 CMOS inverters which are cross-coupled with one another and 2 access transistors which are linked to the correlative bit lines [16]. This configuration is used conventionally. The gates of pass transistor are linked to the write line (WL) and complementary bit lines (BLB and BL) are linked to the write data (available on the data cell) during the write mode and connected to the read data (taken from the data

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cell) during the read mode. The cell design provides lower write delay while the read delay is comparable to other designs [17]. However, during the reading and writing operation, there is a threat to the stability of the design because of the cell being more susceptible to noise which arises due to the operations. Therefore, the structure of the cell needs to be designed carefully so that no change in state occurs for the duration of the read and write modes of operation.

B. AVL-G

In AVL-G technique, or Adaptive Voltage Level at Ground technique, an additional circuitry is inserted to the cell design. This additional circuitry consists of an arrangement of one NMOS and two PMOS transistors that are arranged parallel to each other. The input terminal of the NMOS terminal is connected to an input clock. Ground is linked to the PMOS transistors [18].

AVL-G technique is used to decrease the sub-threshold currents. However, it is able to only partially reduce the gate leakage currents. This reduction is explained here. During the active mode, a switch is used to provide 0V to the ground node and for the duration of inactive mode, the switch provides a raised ground level. This raised ground level is known as a virtual ground. Any rise in the virtual ground will result in lower voltage at the M1 transistor gate-source terminal and gate-drain terminal. It also decreases the M2 transistor gate-drain voltage. This causes steep decline in the gate leakage of both transistors. The gate leakages of M5 and M6 transistors remain unchanged. However, an added gate leakage arises in M5 transistor because of increase of drain voltage in M1. Although conventionally only one transistor is applied to a SRAM cell bank, the present leakage from it is substantially important. This is because its area needs to be much larger when compared with the NMOS transistors that are used. This is done to avoid any degradation of performance in the active mode.

C. AVL-S

In AVL-S technique, or Adaptive Voltage Level at Source technique, additional circuitry is inserted to the cell design. This additional circuitry consists of an arrangement of 1 PMOS transistor connected in parallel with 2 NMOS transistors. An input clock is also connected to the input terminal of the PMOS transistor [18]. AVL-S technique is used to lessen the gate leakage currents. However, the access transistor remains unaffected by two gate leakage currents present in the access transistors and 1 sub-threshold current component. This results in an additional leakage present sub-threshold across the second access transistor. This reduction is explained here. During the active state, V_{DD} is applied to SRAM, whereas in the inactive state, a reduced voltage supply is applied. The drain voltage of M1 and M2 transistors are at V_{DD} due to M4 transistor being in the "ON" state. This result in a lower gate voltage of M1 transistor and consequently the gate currently is steeply lowered. A lower voltage at gate-drain terminal of M2 transistor is observed due to decrease in drain voltage of the same. This causes reduced gate leakage current through it. However, the gate leakage through M5 transistor remains unaltered. When it comes to the sub-threshold leakage currents, there is reduction in M2 and M3 transistors; however, nothing changes in M3 transistor. A reduction in M6 transistors' source voltage implies one EDT leakage component remaining unaltered and one getting reduced. The PMOS transistor results in negligible added leakage current in the AVL-S technique. Hence, it is seen that the AVL-S technique is better than the AVLG technique in terms of having a greater impact on the gate leakage current reduction [19].

D. AVL

The AVL Technique decreased sub-threshold leakage power along with the gate leakage current [20]. AVL circuit consists of one PMOS and two series connected NMOS, which decreases the voltage being applied to the load circuit. A sleep signal controls the AVL circuit. During the low cycle of this sleep signal, PMOS is "ON", while the two NMOS in series are "OFF". We get total voltage from this circuit during this cycle. During the transition of the sleep signal from low to high, the two NMOS connected in series are "ON" and the PMOS is "OFF". This method is used to regulate the circuit / design and is a mixture of the AVL-S method (used to lower the power voltage value) and the AVL-G method (used to produce a virtual ground above 0V).

E. MTCMOS

MT-CMOS or Multi Threshold CMOS logic is an efficient standby leakage control technique [21]. For maximising high stability and minimising power dissipation, the multi threshold logic uses high and low V_{TH} MOS transistors. Between logic circuitry and power supply rails sleep transistors having high V_{TH} are applied. Sleep signals are employed to enable these high V_{TH} sleep transistors. They employ high threshold transistors in order to decrease the power usage in standby state [22]. On the other hand, low threshold transistors are employed to increase stability and performance during active state.

IV. PARAMETERS

A. Static Noise Margin

Static Noise Margin, or thereby referred to as, SNM, is an important figure of merit associated with an SRAM cell. It helps in measuring or determining the strength of an SRAM cell to retain information against that of noise. The lease quantity of voltage noise available in the storage nodes of a cell needed to invert the state of the said cell is known as its SNM [23]. SNM is dependent on the following parameters: (a) Cell ratio or CR, (b) Supply voltage, (c) Pull up ratio or PR.

In terms of the stability, a high SNM is needed. The ratio of the driver-transistor size to the size of the load-transistor is known as the CR[24] for the duration of the read mode. The volume proportion of the end transistor to that of the control transistor is referred to as the PR[24] during the read phase. Mathematically,

During read mode, CR=(W1/L1) / (W5/L5)

During write mode, PR = (W4/L4) / (W6/L6)

SNM is associated with the V_{TH} of PMOS and NMOS components. SNM majorly affects the write and read margins of a cell. Typically, Static Noise Margin and the threshold voltages, or V_{TH}, of the PMOS and NMOS components are in direct proportion with one another. Hence, for increasing the SNM, we need to increase these threshold voltages. However, we can only increase this to a certain level.

This is because if we increase the threshold voltages too much, then the SRAM cells will be too difficult to operate. The reason for this is that it is difficult to flip or invert the operation of these PMOS and NMOS devices. While changing the CR or Cell ratio, various delays are decreased. With the rise in cell ratio, the corresponding size of the driver transistor is also bound to increase, and further, an increase in current also occurs. With this increase in current, the SRAM becomes faster, i.e., its speed increases. By altering the cell ratio, its corresponding SNM is obtained [25]. Hence, we can see that different values of SNM are obtained for different values of cell ratio in various technologies of the SRAM cell.

B. Read Static Noise Margin

Read SNM or RSNM is defined as the SNM observed through the read operation or mode of the cell. It is noticed that the RSNM decreases during the read access. This is because RSNM is ideally calculated while the WL is set to logic ‘1’ or is high and when both the BL and BLB are precharged to ‘1’. During read mode of operation, the access transistor (connected to WL) is set as high, i.e., it is set to ‘1’ and the BL and BLB, both are pre-charged to high, i.e. at ‘1’. Through the access transistor, the internal node of the cell (which is ‘0’), gets pulled up. This voltage increase degrades the SNM for the duration of the read operation; hence the RSNM is reduced [26]. At the onset of a read mode, the data that is stored (‘0’) is flipped to ‘1’ if it is overwritten. This happens because of the process of positive feedback, when the voltage at node V1 equals the V_{TH} of NMOS N1 to pull node V2 down to ‘0’ and in turn pull node V1 upto ‘1’. This leads to reading of incorrect bit when the mode of the cell is being changed. An important FoM (or Figure of Merit) is given by the RSNM [27]. RSNM can be obtained by the graphical representation of the VTC curves of the CMOS inverters used in the SRAM cell. It is deliberated as the length of side of biggest square that fits into the graph, between the two VTCs. Its unit is Volts. If the external DC noise becomes bigger as compared to the RSNM leading to loss in data, the mode of the SRAM cell gets changed. For the duration of the read mode of logic ‘0’, Q=0 and QB=1. In the conventional 6T SRAM cell design, if DC noise is introduced at either Q or QB, the state of the opposed storage node gets inverted and this results in a decrease in the RSNM.

C. Write Static Noise Margin

“Write Static Noise Margin” or “WSNM” is the SNM observed for the duration of the write mode of the cell. The WSN is known as the least bit-line voltage needed to change the mode of the SRAM cell [28]. Throughout the write mode, the information to be stored is forwarded to the bit lines. WL is then triggered. The access transistors are thus turned ON. The bit-line which holds the logic ‘0’ pulls the node of the cell that has the data stored =1 and pulls it to logic ‘0’. This inverts mode of the cell. Since cross coupled inverters are used, they have complementary data; hence their respective Voltage transfer characteristics are obtained using different circuits. To simulate a write logic ‘0’ to a node, the circuit that represents inverter with logic ‘1’ stored and its equivalent bit-line are linked to the ground, While the bit line is linked to ground and WL to V_{DD} or supply voltage, a DC voltage sweep is carried out at V1 and voltage output at V2 is calculated. The WSNM is obtained during the write mode by instigating a linear DC noise at one of the storage nodes and noting the outcome at the other[26].

D. Power Dissipation

Power dissipation is categorized in to the various types, namely, short circuit power, static power and dynamic power [29]. Static power is known as the dissipation due to the CMOS circuit during standby mode. Various leakage components that constitute static power are sub threshold leakage, gate oxide tunneling leakage and reverse bias leakage [30]. Consequently recharging for obtaining faster read access time and the driving of these bit lines increase the power consumed by the SRAM cells further. Low power operation of the system can be obtained by reducing the leakage current which can consequently lower the leakage power consumed. We mainly focus on short circuit power dissipation, delay and area. We analyze several models of SRAM cells by calculating their power dissipation, delay, area and conclude the best among the existing models. For the SRAM cell designs, two aspects are important. They are dynamic energy or power consumption and delay of write and read operation. Dynamic energy consumption is the energy or power consumed all through the modes of the SRAM cell, i.e., read mode and write mode [31]. This establishes the time battery operation in the mobile application. Previous work that has been published mainly focuses on the power modeling, however analytic work has not yet been focused on, which includes delay or power consumption. To reduce the power usage, the response time gets reduced. One effective method to decrease the dynamic power is by lowering the V_{DD} or the supply voltage. This method is observed to lessen the dynamic power by 4 times [32]. It also decreases the leakage power linearly.

E. Delay

The delay during the write and read modes of the SRAM cell establish the speed of the said SRAM. This plays an essential role in the height speed application [33]. Previous work that has been published mainly focuses on the power modeling, however analytic work has not yet been focused on, which includes delay or power consumption.

V. SIMULATIONS

A. Conventional 6T SRAM Cell

Cadence Virtuoso in standard 180nm CMOS technology is employed to implement simulations of 6T SRAM cell. The 6T SRAM has 6 transistors arranged to form 2 inverters and 2 pass transistors. The circuit is shown below.

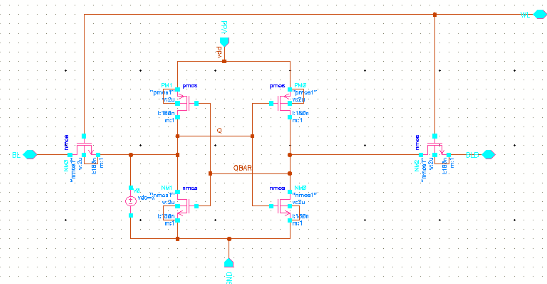

Fig 1: Schematic diagram of a Conventional 6T SRAM Cell

The SNM of an SRAM cell is given by the length of the major square that fits into the butterfly cure. For this purpose, the butterfly curve of the 6T SRAM with conventional design is given. By calculating the length of biggest square, we get the SNM to be 233mV.

Further, the transient analysis of the working of the cell exposes the operations and functioning. Through this, we also get the total power dissipation. The total power consumed is the measurement of the highest peak of total power as shown in the figure below. For a conventional 6T SRAM cell, it comes out to be 405.3 µW.
Further, analysis of the total delay of a conventional SRAM cell is carried out using Cadence. The delay is found out to be 2.488*10-9 as shown below.

B. AVL with Controlled Input

Cadence Virtuoso in standard 180nm CMOS technology is used to implement simulations of conventional 8T SRAM with controlled input as proposed in the base paper "Improved Speed Low Power and Low Voltage SRAM Design for LDPC Application Circuits". The 8T SRAM with controlled input consists of 8 transistors that use pass transistor logic along with dynamic logic in order to get more efficient with respect to latency, overall performance, power consumption and SNM; thereby increasing the overall efficiency. The schematic diagram of the 8T SRAM cell with controlled input is seen in the figure below.

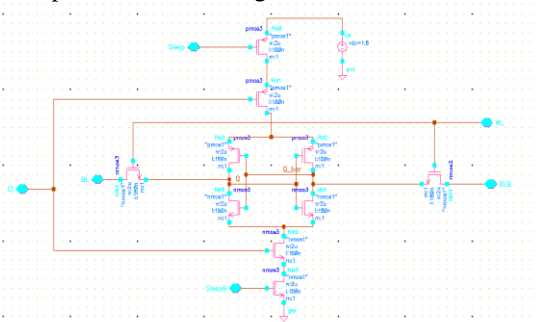

Fig 2: Schematic diagram of an AVL SRAM Cell with Controlled Input

The SNM of an SRAM cell is given by the length of the major square that fits into the butterfly cure. For this purpose, the butterfly curve of the 8T SRAM with controlled input is given. By calculating the length of biggest square, we get the SNM to be 435mV.

Further, the transient analysis of the working of the cell exposes the operations and functioning. Through this, we also find the total power consumed. The total power dissipation is the value of the highest peak of total power as shown in the figure below. For a conventional 6T

SRAM cell, it comes out to be 402.8 µW.

C. AVL-G 8T SRAM Cell

Cadence Virtuoso in standard 180nm CMOS technology is used to implement simulations of the proposed 8T SRAM with controlled input using AVL-G technology. The AVL-G technology, or Adaptive Voltage Level Ground technology, aims to diminish the leakage current and consequently the power consumed. The schematic of the AVL-G 8T SRAM cell with controlled input is shown in the figure below.

The SNM is given by the length of the major square that fits in the butterfly cure. For this purpose, the butterfly curve of the AVL-G 8T SRAM with controlled input is given. By calculating the length of biggest square, we get the SNM to be 453mV.

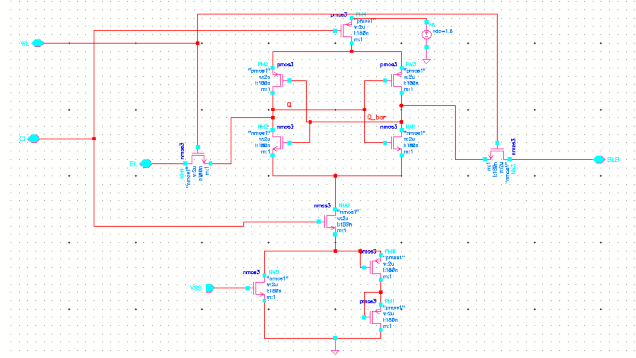

Fig 3: Schematic diagram of a AVL-G 8T SRAM Cell

Further, the transient analysis of the working of the cell exposes the operations and functioning. Through this, we also get the total power dissipation of the cell. The total power dissipation is the value of the highest peak of total power as shown in the figure below. For a conventional 6T

SRAM cell, it comes out to be 358.4 µW.

D. AVL-S 8T SRAM Cell

Cadence Virtuoso in standard 180nm CMOS technology is used to implement simulations of the proposed 8T SRAM with controlled input using AVL-S technology. The AVL-G technology, or Adaptive Voltage Level Source technology, aims to diminish the leakage current and consequently the power consumed. The schematic of the AVL-S 8T SRAM cell with controlled input is shown in the figure below.

The SNM is given by the length of the major square that fits into the butterfly cure. For this purpose, the butterfly curve of the AVL-S 8T SRAM with controlled input is given. By calculating the length of biggest square, we get the SNM to be 475mV. Further, the transient analysis of the working of the cell exposes the operations and functioning. Through this, we also get the total power consumed by the cell. The total power dissipation is the value of the highest peak of total power. This is seen in the following figure. AVL-S 8T SRAM with controlled input, it comes out to be 159.05 µW.

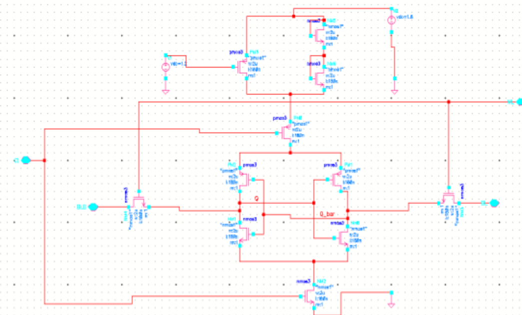

Fig 4: Schematic diagram of an AVL-S 8T SRAM Cell

E. AVL 8T SRAM Cell

Cadence Virtuoso in standard 180nm CMOS technology is used to implement simulations of the proposed 8T SRAM with controlled input using AVL technology. The AVL technology, or Adaptive Voltage Level technology, aims to decrease the leakage current and consequently the power consumed. It combines both the AVL-S technology and AVL-G technology thereby making the circuit more

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efficient. The schematic of the AVL 8T SRAM cell with controlled input is shown in the figure below.

The SNM is given by the length of the major square that fits into the butterfly cure. For this purpose, the butterfly curve of the 8T SRAM with controlled input is given. By calculating the length of biggest square, we get the SNM to be 519mV.

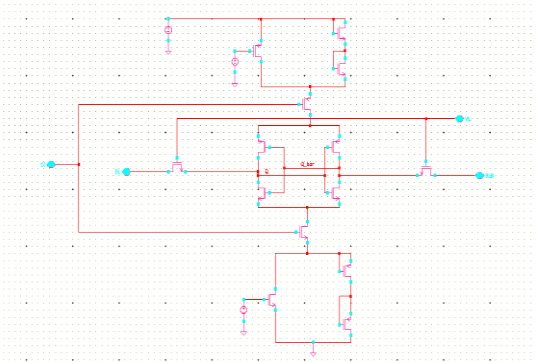

Fig 5: Schematic diagram of an AVL 8T SRAM Cell

Further, the transient analysis of the working of the cell exposes the operations and functioning. Through this, we also get the total power consumed by the cell. The total power dissipation is the value of the highest peak of total power as shown in the figure below. For AVL 8T SRAM with controlled input, it comes out to be 87.48 µW.

F. MT-CMOS SRAM Cell

Cadence Virtuoso in standard 180nm CMOS technology is used to implement simulations of the proposed 8T SRAM with controlled input using MT-CMOS technology. The MT-CMOS technology, or Multi Threshold CMOS technology, aims to optimize power and delay. The schematic of MT-CMOS 8T SRAM cell with controlled input is revealed in the following figure.

The SNM is given by the length of the major square that fits into the butterfly curve. For this purpose, the butterfly curve of the MT-CMOS 8T SRAM with controlled input is given. By calculating the length of biggest square, we get the SNM to be 468mV.

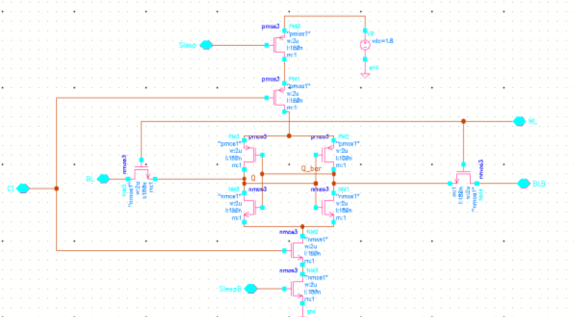

Fig 6: Schematic diagram of a MT CMOS SRAM Cell

Further, the transient analysis of the working of the cell exposes the operations and functioning. Through this, we also get the total power dissipation. It is defined as the measurement of the highest peak of total power as shown in the figure below. For a MT-CMOS 8T SRAM cell with controlled input, it comes out to be 313.18 µW.

VI. RESULT

A. Static Noise Margin

SNMs found of various SRAM cells in standard 180nm CMOS Technology using the Butterfly curve (graphical method) obtained by simulation on Cadence Virtuoso is compiled in the table below:

Technology	SNM (in mV)	Percentage Increase
Conventional 6T SRAM cell	233	-
8T SRAM cell with Controlled Input	435	86.69%
AVL-G 8T SRAM with Controlled Input	453	94.42%
AVL-S 8T with Controlled Input	475	103.63%
AVL 8T SRAM with Controlled Input	519	122.75%
MT-CMOS 8T with Controlled Input	468	100.86%

Fig :

As seen from the Table, the Highest SNM is shown by 8T SRAM with Controlled Input using AVL technology, which is 122.75% more than conventional 6T SRAM.

B. Total Power Dissipation

The total power dissipation of various SRAM cells in standard 180nm CMOS Technology using the transient analysis obtained using simulation on Cadence Virtuoso are compiled in the following table:

Technology	Power Dissipation (in µW)	Percentage Decrease
Conventional 6T SRAM cell	405.3	-
8T SRAM cell with Controlled Input	402.8	0.62%
AVL-G 8T SRAM with Controlled Input	358.4	11.57%
AVL-S 8T with Controlled Input	159.05	60.76%
AVL 8T SRAM with Controlled Input	87.48	78.42%
MT-CMOS 8T with Controlled Input	313.18	22.73%

Fig :

As seen from the Table, the lowest Total Power Dissipation is shown by 8T SRAM with Controlled Input using AVL technology, which is 78.42% less than conventional 6T SRAM.

C. Delay

The Delay found of the SRAM cells in standard 180nm CMOS Technology obtained by simulation on Cadence Virtuoso is compiled in the table below:

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Technology	Delay ($*10^{-9}$)	Percentage Decrease
Conventional 6T SRAM cell	2.488	-
8T SRAM cell with Controlled Input	2.008	19.29%
AVL-G 8T SRAM with Controlled Input	1.982	20.34%
AVL-S 8T with Controlled Input	1.56	37.30%
AVL 8T SRAM with Controlled Input	1.0	59.8%
MT-CMOS 8T with Controlled Input	1.62	34.89%

From the above table, we can see that the lowest delay is shown by 8T SRAM with Controlled Input using AVL technology, which is 59.8% less than conventional 6T SRAM.

D. Comparision analysis

Different SRAM cells in standard 180nm CMOS Technology are obtained by simulation on Cadence Virtuoso. They are compared using different parameters such as SNM (Static Noise Margin), Total Power Dissipation and Total Delay and are consequently compiled in the table below:

Technology	SNM (in mV)	Power Dissipation (in µW)	Delay ($*10^{-9}$)
Conventional 6T SRAM cell	233	405.3	2.488
8T SRAM cell with Controlled Input	435	402.8	2.008
AVL-G 8T SRAM with Controlled Input	453	358.4	1.982
AVL-S 8T with Controlled Input	475	159.05	1.56
AVL 8T SRAM with Controlled Input	519	87.48	1.0
MT-CMOS 8T with Controlled Input	468	313.18	1.62

VII. CONCLUSION

SRAM cells play crucial roles in memory design systems to achieve low power, high speed and high performance. For making SRAM more efficient, the future SRAM technologies need to focus on the optimization from both the testing front and the circuit design front.

In this paper, many research papers on the Static Noise Margin of SRAM were reviewed and thereafter formulated in the review table. We found that different topologies of SRAM cells have different SNMs, power dissipation and total delay. Further, it was seen that different technologies can be used to increase the overall efficiency. The simulations of the 6T SRAM cell with conventional design, the 8T SRAM cell with Controlled Input, AVL-G 8T SRAM cell with Controlled Input, AVL-S 8T SRAM cell with Controlled Input, AVL 8T SRAM cell with Controlled Input and MT-CMOS 8T SRAM cell with Controlled Input have been analyzed effectively using Virtuoso Cadence on 180 nm technology. The compared parameters are static noise margin, Total Power Dissipation and Total Delay.

After the analysis we see that by increasing the numbers of transistors read and write delays and leakage power consumption is increased as the cell area increases. Consequently, new technologies were introduced to 8T SRAM with Controlled Input like AVL-G, AVL-S, AVL and MT-CMOS. The aim is to decrease the power dissipation, increase the SNM and decrease the total delay. The most efficient of all technologies used was AVL with 8T SRAM Controlled Input.

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