Low Power Design of 2–4 and 4–16 Line Decoders

Grande NagaJyothi, Gorantla Anusha, Kundu Debanjan

***Abstract*: Here, we are proposing a novel design of 2:4 decoder and 4:16 decoders which are designed by using line decoder concept. By using proposed design, the area and power consumption of 2:4 decoder and 4:16 decoder can be reduced. In the existing work they have used DVL (Dual Value Logic) and Transmission gate Logic to implement a 14-Transistor 2:4 decoder for minimizing the transistor count. By using 2:4 pre-decoders and post-decoders they implemented 4:16 decoders. Mixed logic is also used for this purpose. Here we have implemented a single 2:4 decoder with minimum transistor count and low power consumption which is used to design a 4:16 decoder. We implement the proposed design in Cadence Virtuoso simulation at 90nm technology and calculated the power and area.**

***Index Terms*: Decoder, inverter, mixed logic, Transmission logic**

I. INTRODUCTION

Static Complementary Metal Oxide Semiconductor circuits are used for most logic gates in integrated circuit (IC) design [1-3]. They consist of pull-down and pull-up networks which provides good performance along with R/N ratio (R-resistance and N- Noise) and device variation. Therefore, CMOS logic is described by robustness against transistor sizing and voltage scaling and thus reliable operation at small transistor sizes and low voltages. Pass transistor logic (PTL) is grown up to give an alternative chance to CMOS logic, which can improve speed, power, and area [4]. The difference in the design is that, both the gates are connected to the inputs along with source/drain terminals of transistors. Series PMONS-NMOS or parallel combination of PMOS-NMOS used for realizing PT. Parallel combination of PMOS-NMOS called transmission gates. Line decoders are mostly used in the peripheral circuitry of memory arrays of the fundamental circuits.

II. DESCRIPTION OF LINE DECODER CIRCUIT

Binary codes are used to represent discrete quantities of information, in digital system. 2n distinct coded elements can be formed using an n bit binary input. The combinational circuit is capable of converting binary information from n bit inputs to a maximum of 2n unique output lines. It can have less than 2n outputs, if the n bit coded information has any unused combinations. The circuits under consideration here are n:m decoders, which has m = 2n min terms of n input.

A. 2:4 Decoder: A 2:4 decoder creates four terms D_0–D_3 from two input variables *A* & *B*. Table- I shows the summary of the logic operation of the basic decoder.

Table-I

A	B	D_0	D_1	D_2	D_3
0	0	**1**	0	0	0
0	1	0	**1**	0	0
1	0	0	0	**1**	0
1	1	0	0	0	**1**

Truth Table of 2:4 decoders

Based on the combination of the input values, one of the 4 outputs which is selected and set to logic 1. Whereas the other values are set to logic 0. Complementary min terms (I0-I3) are generated for an inverted 2:4-line decoder. In case of inverting decoder, the selected output is set to logic 0 and the rest are set to logic 1, as shown in Table II. NAND & NOR gates are given priority over AND & OR gates for designing conventional design of CMOS. This is because, if we use NAND & NOR, we need only 4 transistors, whereas 6 transistors are required for AND & OR based CMOS design. This clearly reduces the number of transistors, which in turn reduce design area, which is one of the most important PPA aspect of digital design. 2 INV & 4 NOR gates are required to design a 2:4-line decoder, shown in Fig. 1(a). Whereas 2 INV & 4 NAND are sufficient for designing inverting decoder. No extra transistors are required for inversion of result. Fig. 1(b) shows the inverting line decoder. 20 transistors will be yield from both line & inverting line decoders.

Table-II

A	B	I_0	I_1	I_2	I_3
0	0	**0**	1	1	1
0	1	1	**0**	1	1
1	0	1	1	**0**	1
1	1	1	1	1	**0**

2:4 Inverting decoder truth table

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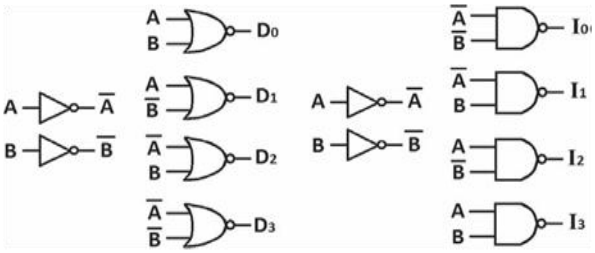

Fig.1(a) Fig.1(b)

Fig.1 Twenty transistor 2:4-line decoders realized with CMOS 1(a) Non-inverting decoder using NOR 1(b) Inverting decoders using NAND

B. 4:16 Line Decoder using 2:4 Pre-decoders:

16 min terms range from D0 to D15 are generated from a 4:16 line decoder, which takes 4 input variables *A*, *B*, *C*, and *D*. Pre decoder circuits ate used as the first stage of the 2-level decoder circuit. 1st level pre-decoding technique is such that, blocks of n address bits can be pre-decoded into 1:2n pre-decoded lines, which are taken as inputs to the final stage of the decoder. Hence, a 4:16 decoder can be realized using two 2:4 inverting decoders and sixteen 2-input NOR gates. 104 transistors will be yield, if the decoder is implemented using CMOS logic, which require eight INVs and twenty-four gates of 2-input.

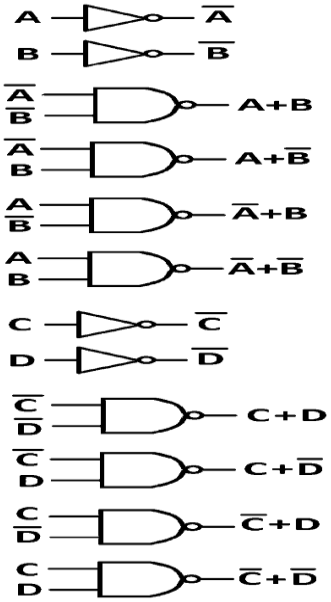

Fig.2 (a) Line Decoder using two 2:4 inverting Pre-decoder

III. MIXED LOGIC DESIGN

Line decoders can be implemented by using Transmission gate logic (TGL) [5-6] which are used for realizing AND/OR gates. Fig. 3(a) and (b) respectively shows 2-input AND/OR gates using TGL logic. These circuits swing to the full, but do not restore for all combinations of input data. As per Pass Transistor Logic (PTL), there are mainly two circuit styles; which uses nMOS pass transistor circuits only. For this 3T AND/OR gates are taken into consideration. They are (a)AND gate using TGL. (b) OR gate based on TGL. (c) AND gate using DVL. (d) OR gate based on DVL. In our research work, we have considered DVL (Dual Value Logic), which preserves controlled transistors count with full swing operation. Fig. 3(c) and 3(d) shows two-input AND/OR gates with Dual Value Logics. They are non-restoring but swings to the fullest. TGL/DVL requires only 3T for restoration, if the available inputs are complemented. Transistors count can be reduced by using TGL/DVL logics, because decoders are high fanout circuits and few inverters can be used by multiple gates. The most important common property of these gates is the asymmetric nature of the circuits, which means non presence of balanced input load. In TGL gates, all 3 transistors are controlled by input X, while input Y crawled to the output through the TG. In case of DVL, two transistor gate terminals are controlled by input X. Input Y controls one gate terminal and passed through a PT to the output. X & Y respectively are referred as the control signal and propagate signal of the gate. Since, INV adds propagation delay in the data path, it's not a good idea to use complementary inputs as the propagation signal.

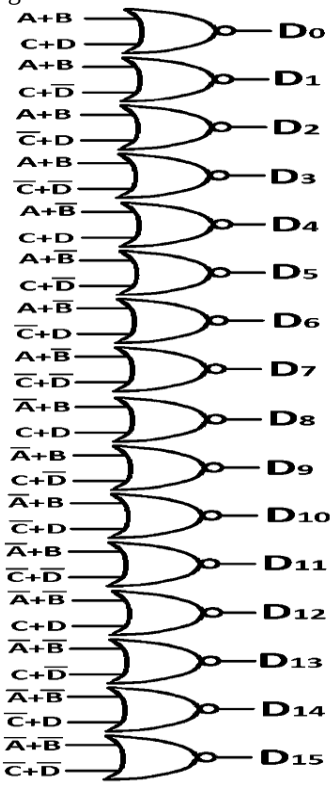

Fig. 2(b) Post-decoder using NOR

IV. 14T 2:4 LOW-POWER TOPOLOGY

Total 16T are required for designing a 2:4-line decoder using either of TGL or DVL. Out of total 16T, there are 12 AND/OR gates and rest are INVs. However, it is possible to eliminate one of the two INVs, by mixing up both AND gates into the same topology and by making proper signal arrangements, resulting into lower transistor count to 14. Let us consider that, out of the two input signals, namely, A & B, we aim to eliminate B from the circuit. Using DVL, D0 is implemented and A is used as propagate signal. Whereas, D1 is realized using TGL gate, where B propagates signal. Then, D_2 is designed with a DVL gate, and A propagates signal. Finally, TGL implement D3 and B is used

for signal propagation. The TGL-DVL combination helps to avert the complementary of B signal and hence B inverter can be omitted from the circuit, which helps to result in a 14T topology consisting 5 pMOS and 9 nMOS. Using the same methodology, OR based 2:4 inverting line decoders can be implemented with 14 transistors (9 pMOS and 5 nMOS). I0 and I2 are implemented with TGL (when B is used as the propagate signal) and I1 and I3 are implemented with DVL with signal A as the propagates signal. In the same manner, again B can be excluded. This controlled reduction of inverters pulls the transistor count down. It also reduces overall switching activity and logical effort of the circuits, which in turn reduce the dissipation of switching power. The proposed new topologies are termed as "2:4 LP" and "2:4 LPI". "LP" stands for "low power" and "I" for "inverting." Fig. 4(a) & (b) represent the schematics of 2:4 LP and 2:4 LPI respectively.

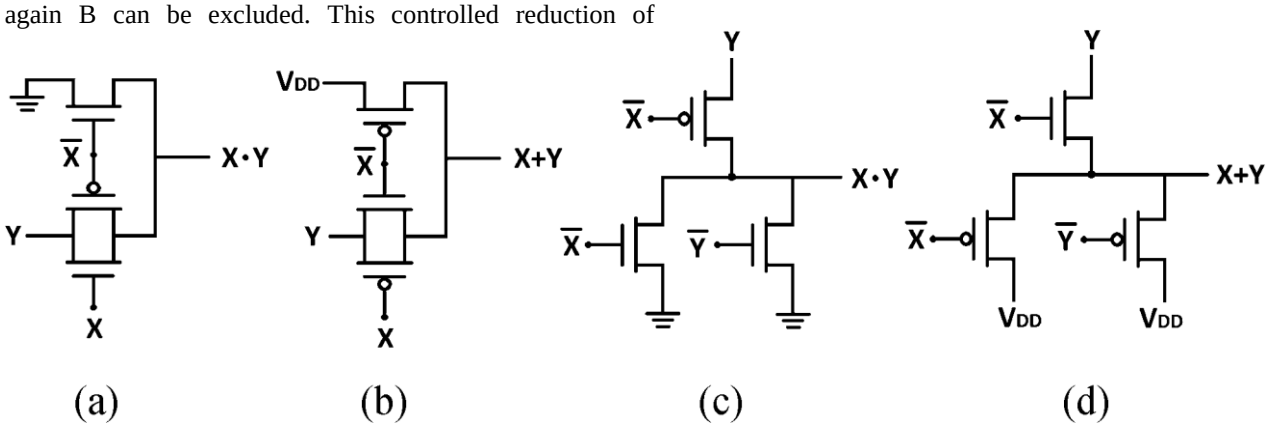

Fig. 3 AND/OR gates using 3T (a)AND gate using TGL. (b) OR gate using TGL. (c) DVL based AND gate. (d) DVL based OR gate

V. PROPOSED DESIGN

In the previously designs, the 2:4 decoder output D_0 and D_2 logic was made using CMOS logic and output D_1 and D_3 was made using transmission gate logic. The total transistor count was 14. In the proposed design, we have used pass transistor logic for both D_0 & D_2 and D_1 & D_3 are made using transmission gates. So, the transistor count is reduced to 12.When constructing 4:16 decoder using 2:4 decoder, we used 2:4 pre-decoder and conventional CMOS logic NOR gates. For designing NOR gate by using CMOS, we need four transistors. So, for total 16 NOR gates, we need 16x4=64 transistors. Here, in this design, we have used new 2:4 pre-decoders and pass transistor logic NOR gates. Using pass transistor logic we just need two transistors to make a NOR gate. So, total 16x2=32 transistors will be needed. So, total number of transistors needed to design 4:16 decoder is getting reduced rapidly. The schematic and power and transient analysis of both the proposed 2:4 decoder and 4:16 decoders are shown from fig.5 to fig.10.

VI. SIMULATION RESULTS

The proposed 2:4 decoder and 4:16 decoders are implemented in cadence virtuoso 90nm technology. The circuit diagram and simulation results of 2:4 decoder and 4:16 decoders are shown from figure.5 to figure.10. From table III we can analyze the power consumption and area of the proposed and existing designs. Area and power consumption occupied by the 2:4 proposed decoder is reduced when compare with the existing 2:4 decoder. Also the area and power consumption of proposed 2:4 inverter decoder is reduced when compare with existing design.

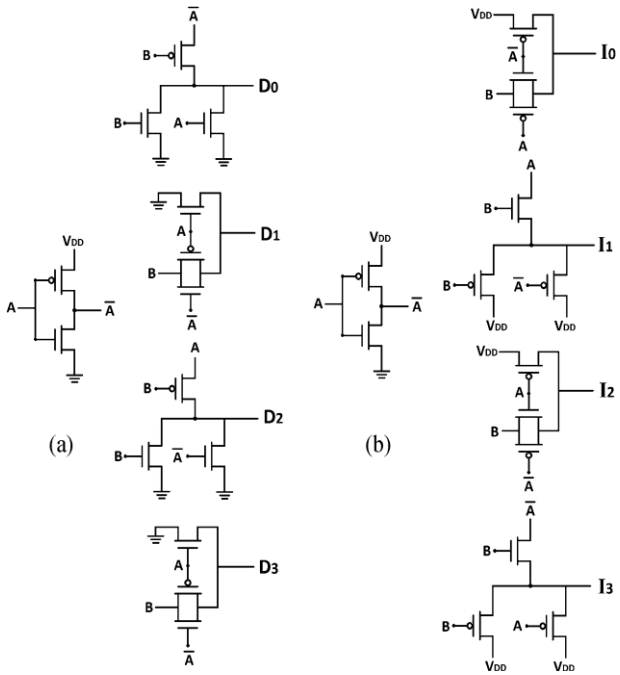

Fig.4 Novel 14T 2:4-line decoders (a) 24LP. (b) 2:4LP

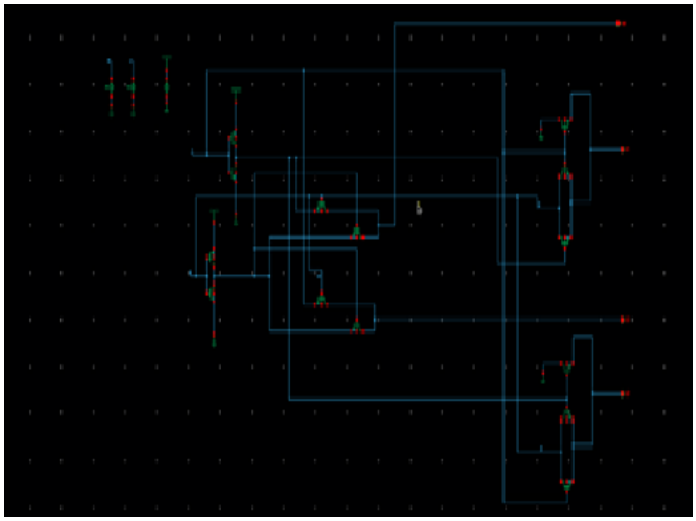

Fig.5 Proposed 2:4 decoder

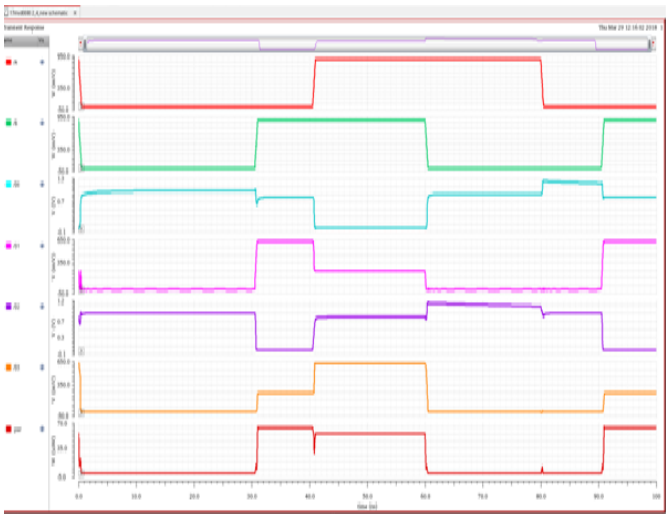

Fig.6 Transient and power analysis

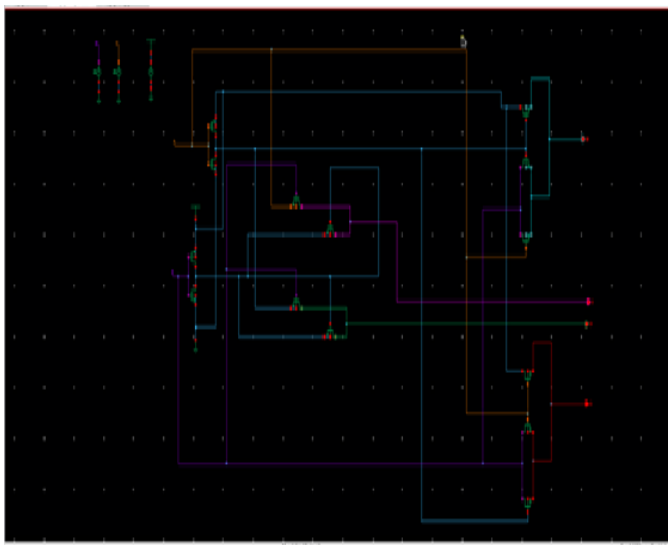

Fig.7 Proposed 2:4 inverting decoder

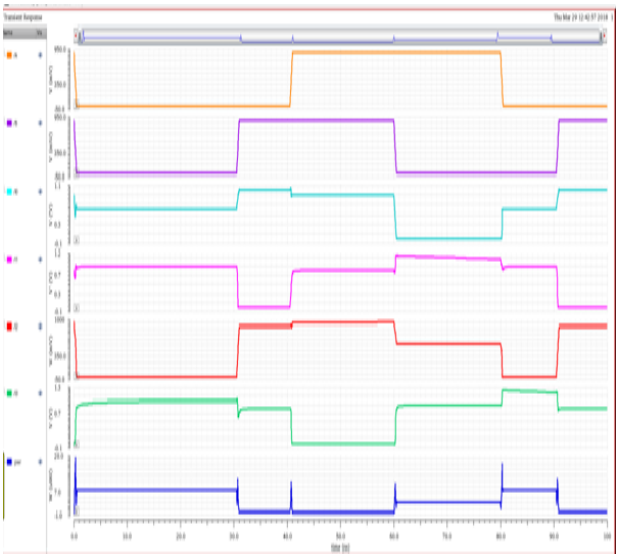

Fig.8 Transient and power analysis

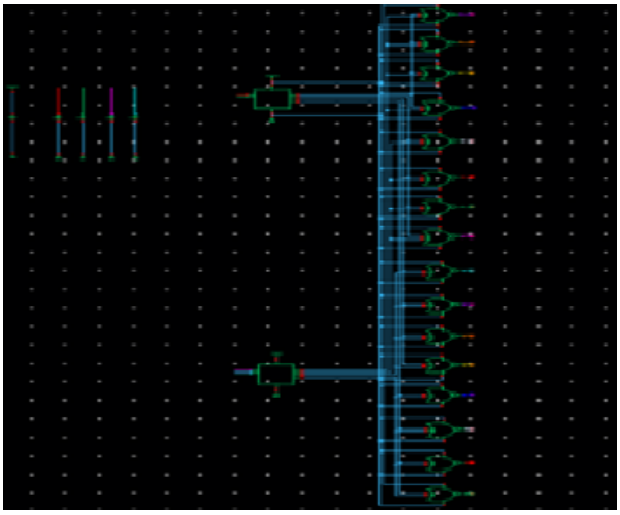

Fig.9 Proposed 4:16 decoder

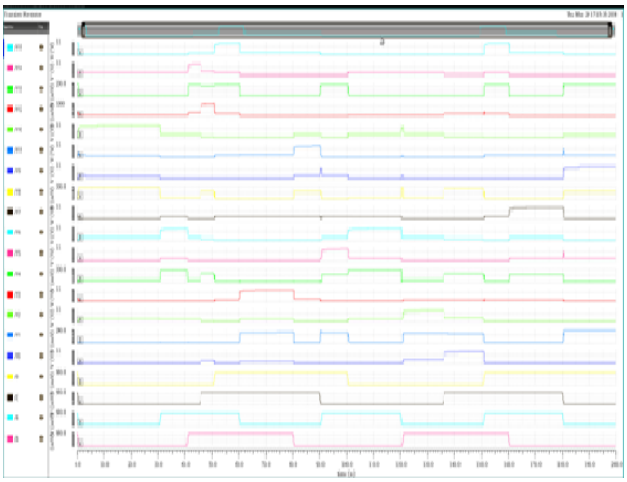

Fig 10 Transient and power analysis

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Table III

	2-4 DECODER	2-4 DECODER PROPOSED	2-4 INVERTING DECODER	2-4 INVERTING DECODER PROPOSED	4-16 DECODER	4-16 DECODER PROPOSED
POWER (uW)	80.943	63.83	30.086	17.056	416.089	217.84
AREA (no. of transistor)	14	12	14	12	92	56

Area and power consumption results of proposed and existing designs

VII. CONCLUSION

From the proposed design we can conclude that the area i.e. the transistor count is getting reduced. The power consumption of proposed design has 52.61% less than the existing 2:4 decoder and it has 39.13% area savings. The only drawback of proposed design is that because of pass transistor logic, we are not getting the full output voltage swing. But, as a whole the proposed 2:4 and 4:16 design is helpful for low power applications.

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