Implementation of a Solar based Seven Level Asymmetrical Multilevel Inverter Topology with reduced device count

Abeera Dutt Roy, ChandrahasanUmayal

Abstract: A multilevel inverter with half bridge cells and seven switches is implemented for Solar PV based applications. The photovoltaic panels are employed to replace the DC sources and maximum power is ensured by employing a boost converter andPerturb and Observe(P&O) algorithm. The generation of switching pulses is carried by usingNearest Level Control(NLC) technique.The operating principle of the proposed multilevel inverter(MLI) is verified by utilizing different loads and the experimental results are obtained through prototype testing.

Index Terms:Asymmetrical,Cascaded H-bridge, Half bridge, Perturb and Observe,Nearest Level Control(NLC)

I. INTRODUCTION

The main components of renewable energy are Solar, wind and hydro. Compared to other renewable sources available, the solar energy and wind energy have gained more prominence[1]. The solar energy has various advantages like reduction of cost, does not cause pollution and it is available constantly throughout the daytime. MLI combined with solar PV systems is utilized in standalone as well as grid connected systems[2,3].

MLIs are classified as (1)Flying Capacitors (FCs),(2)Neutral Point Clamped (NPC) and (3)Cascaded H-Bridge (CHB). Among all these topologies, CHB possesses various advantages like high modularity and ability to reach medium output voltage levels with the help of low-voltage components [5-8]. These structures are composed of a series connection of several single-phase H-Bridge inverters. The cascaded multilevel inverter can be divided into symmetric and asymmetric forms based on the magnitudes of the DC sources[9-11]. In symmetric form, the DC sources have equal values and these offer modularity and the option to extend the capacity. And the asymmetric structure has unequal values but has the option of increasing the voltage levels with the same component count[12]. The major issue in multilevel inverters is the proportionate increase in the count of the semiconductor devices employed with increase in the number of levels, whereby leading to increased cost of the system. In recent years, researchers have also developed a large number of topologies with reduced component count[13-15]. The MLIs utilizing lesser number of devices and operating at lower switching frequency helps in improving the efficiency of PV inverter which are used for standalone applications.

The maximum power can be obtained from PV by using a suitable MPPT algorithm. The two primary parameters which influence the voltage generated from the solar areIrradiation and temperature[16, 17].

In the literature, various MPPT techniques are available and among them the P&O algorithm is used in this paper.

Anovel seven level cascaded MLI topology using reduced devices is presented. The proposed MLI is synthesized by combining H-bridge inverter and half bridge module. A boost converter along with P&O algorithm ensures maximum power from the PV which is used as a source of the proposed MLI. A prototype is developed which provides the experimental results to confirm the working principle of this architecture.It has the following advantages: (i)considerable reduction in component count (ii)marginal reduction in the requirement of DC sources (iii)reduced switching and conduction losses(iv)compact in size (v)Capability to produce negative voltage levels without a separate H-bridge inverter at the output.

II. MODELLING OF PV

In the proposed work, the PV arrayis usedwhose parameters are provided in the table- I. The PV cell shown in Fig is represented by a current source which is placed in parallel with diode and two resistances are added (a series and shunt resistance).The mathematical model for this array is as follows[19]:

$$I_{pv} = I_{ph} - I_0(e^{\frac{(V_{pv}+R_{se}I_{pv}}{V_T}} - 1) - V_{pv} + \frac{R_{se}I_{pv}}{R_{sh}} \quad (1)$$

Where

I_{pv} = PV cell output current

V_{pv} = PV cell outputvoltage

I_0 = saturation current

$V_T = nKT/q$ = thermal voltage(n = emission coefficient factor of PV cell)

R_{se} =series resistance

R_{sh} = shunt resistance

K = Boltzmann constant

T = cell temperature

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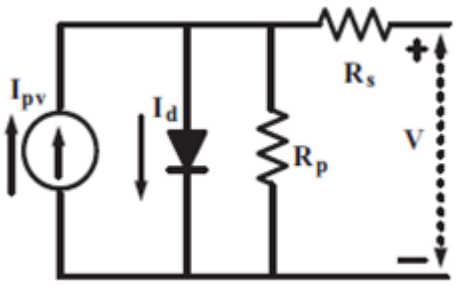

Fig. 1: Equivalent circuit of PV cell

III. PROPOSED PV BASED MULTILEVEL INVERTER TOPOLOGY

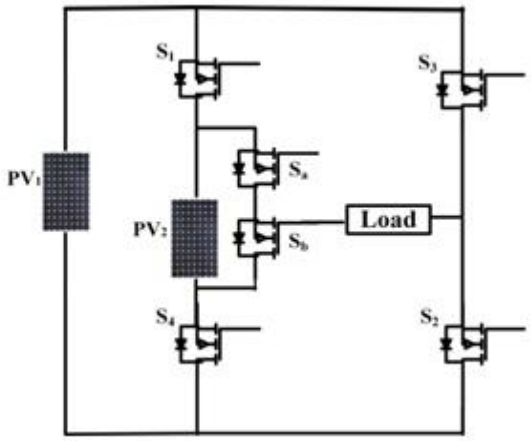

Fig. 2:Circuit of proposed topology for 7-level inverter

The power circuit of proposed MLI is shown in Fig. (**1**). The proposed MLI consists of two voltage sources with the ratios of 1:2((**V_1**=100V, V_2= 200V).The H-bridge module of the topology consists of four MOSFET with antiparallel diodes(S_1,S_2,S_3 and S_4) . The half bridge module of the MLI consists of two MOSFET switches with antiparallel diodes(S_a,S_b) as shown in Fig. 1.A resistive load and combination of resistive and inductive loads are used to validate the performance of the MLI. The circuit shown in Fig. 1can be generalized for higher voltage levels by introducing suitable number of voltage sources and half bridge modules in betweenS_1 and S_4. It is observed from Fig.1 that switch combinations of S_1, S_4 and S_3, S_2 should not be turn on simultaneously to avoid the sources from being short circuited. The different switching states of the seven level inverter where 1 and 0 signify ON and OFF states of the devices are shown in Table I. The Figs. 2 to 9 portray the operating modes to extract various levels of the output voltage. It highlights the usage of only three devices to generate the output voltages whereas the conventional cascaded structure uses 6 devices. This leads to the reduction of power dissipation and the switching losses. The various power components required for this topology is illustrated in Table II.

Table I. Switching States of Proposed Topology

Voltage Level	**S_1**	**S_2**	**S_3**	**S_4**	**S_a**	**S_b**
V_1	0	0	1	1	0	1
V_2	0	1	0	1	1	0
(V_{1+} V_2)	0	0	1	1	1	0
0	0	1	0	1	0	1
0	1	0	1	0	1	0
-V_1	1	1	0	0	1	0
-V_2	1	0	1	0	0	1
-(V_{1+} V_2)	1	1	0	0	0	1

Table II. Required power components for the proposed topology

Parameters	**Values**
Count of Output levels	$2^{n+1}-1$
Total count of switches	$2n+1$
Maximum value of output voltage	$(n-1)$ V_{dc}
PIV	(4/7) V_{dc}
Number of On state switches	$(n-1)$+3

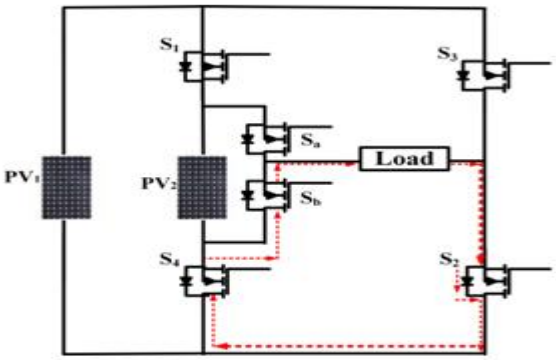

Fig.3 Mode 0

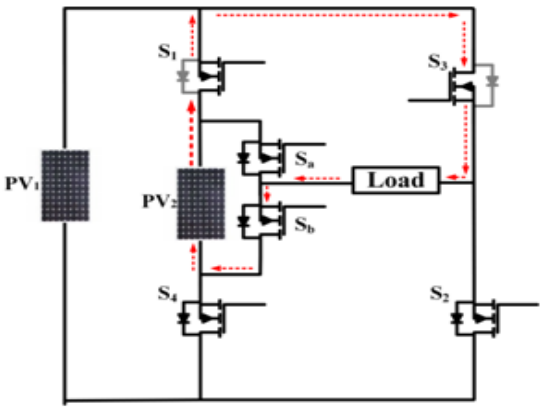

Fig.4 Mode 1

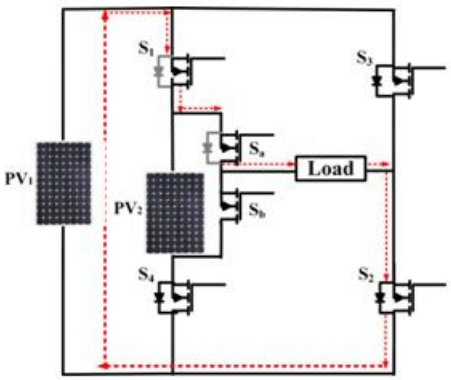

Fig.4 Mode 2

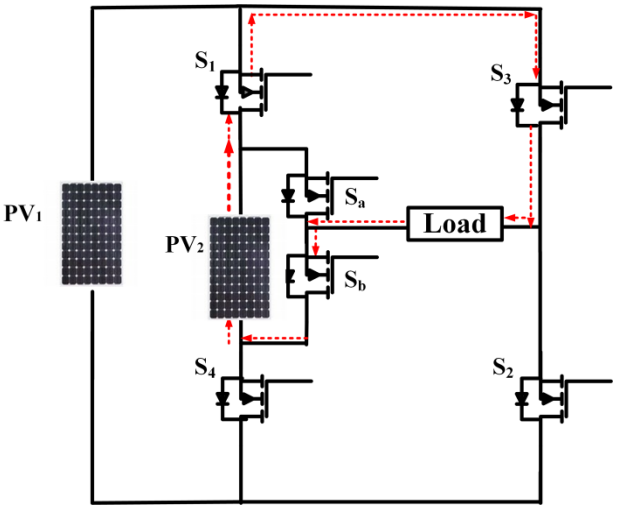

Fig.5 Mode 3

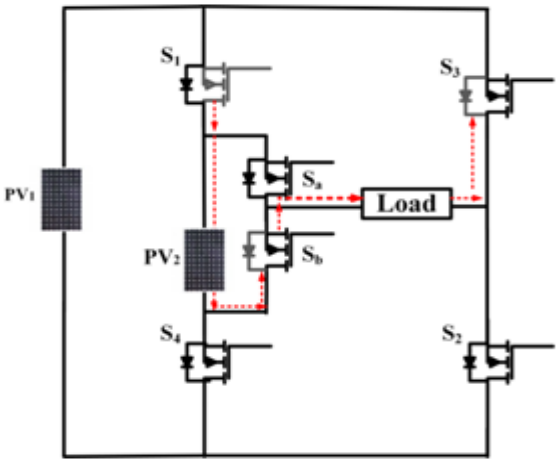

Fig.6 Mode 4

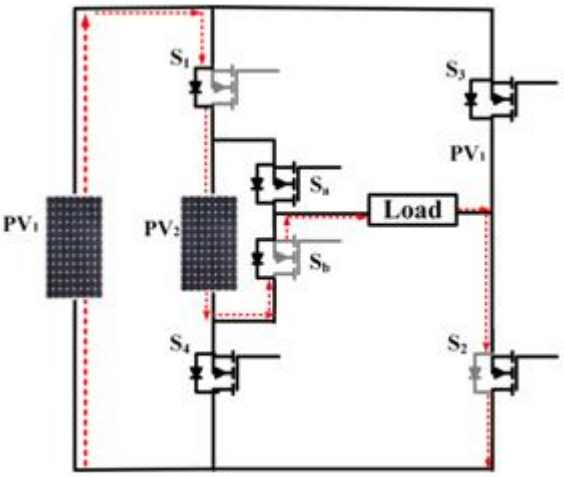

Fig.7 Mode 5

IV. MPPT CONTROL

Nowadays, MPPTis very common to extract maximum power from PV panels[17]. Irradiation and temperature are the two major factors which affect the generated voltage from PV system.]. It also helps to maintain optimum performance of the system when there are deviations in the climatic conditions or Standard Test Condition values[18]. The P&O algorithm is used for the proposed topology which is shown in the Fig. 8.

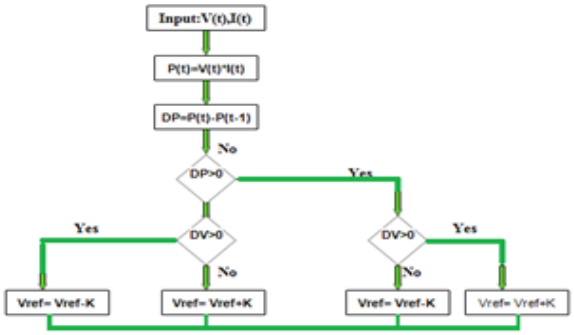

Fig. 8: Algorithm of P&O

This algorithm is instrumental in changing(i.e. increasing or decreasing) the current or voltage at regular intervals and the present power is compared with the previousiterative power to maximize the output power. If an increase in the output power is observed, then the voltage perturbation occurs in the same direction otherwise the perturbation should be carried out against the initial direction. The advantage of this method is when the speed of execution of the P&O increases, then the losses incurred by the system reduces.

V. DESIGN OF BOOST CONVERTER

As the primary source of the proposed configuration is PV Module, it delivers variable and intermittent power which infers reduced power transfer to the load.

Hence in such variable and intermittent power source needs impedance matching between the source and load for maximum power transfer[19,20]. The boost converter is introduced to match impedance for maximum power transfer and the circuit diagram of the same is provided in Fig 9.

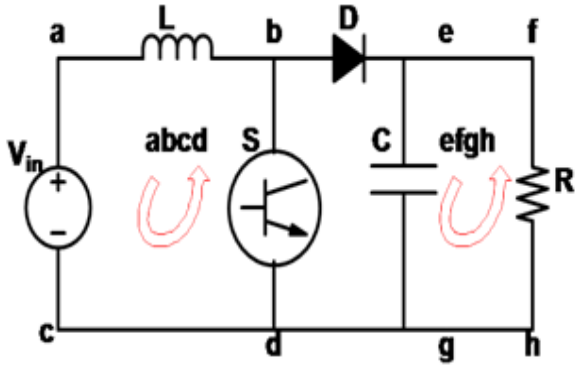

Fig. 9: Boost converter

The State and Output equations at DT mode is obtained by applying KVL on loop abcd

$$\frac{di_L}{dt} = \frac{V_{in}}{L} \quad (1)$$

BY applying KVL on loop efgh

$$\frac{dVc}{dt} = \frac{iC}{C} \quad (2)$$

But the capacitor voltage delivers the load current,

$$\text{hence} i_c = -il_{oad} = \frac{V_0}{R} \quad (3)$$

Now equn (2) can be rewritten as

$$\frac{dVc}{dt} = \frac{iC}{C} = -\frac{V_0}{RC} \quad (4)$$

Now state equns can be rewritten in matrix form as,

$$\begin{bmatrix} i_L' \\ V_c' \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ V_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} [V_{in}] \quad (5)$$

$A_1 B_1$

Now the output equation is given by,

$$V_0 = [0 \quad 1] \begin{bmatrix} i_L \\ V_c \end{bmatrix}$$

C_1

(6)

State and Output equations at (1-D)T mode

By applying KVL on loop abehdc

$$V_{in} = V_L + V_c \quad (7)$$

$$V_{in} = L\frac{di_L}{dt} + V_c \quad (8)$$

$$\frac{di_L}{dt} = \frac{V_{in}}{L} - \frac{V_c}{L} \quad (9)$$

By applying KCL on node e

$$i_{L=i_c} + i_{load} \quad (10)$$

$$i_L = \frac{CdV_c}{dt} + \frac{V_c}{R} \quad (11)$$

$$\frac{dV_c}{dt} = \frac{i_L}{C} - \frac{V_c}{RC} \quad (12)$$

Now state equations can be rewritten in matrix form as,

$$\begin{bmatrix} i_L' \\ V_c' \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ V_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} [V_{in}]$$

A_2 B_2

(13)

And the output equation is given by

$$[V_c]$$

C_2

(14)

In this paper, circuit averaging is applied to compute state and output matrices. Hence,

$$A = A_1 D + A_2 D(1 - D) \quad (15)$$

$$B = B_1 D + B_2 D(1 - D) \quad (16)$$

$$C = C_1 D + C_2 D(1 - D) \quad (17)$$

Now, substituting the value of A_1, B_1, C_1, A_2, B_2, C_2 from equations 5,6, 13, 14

$$\begin{bmatrix} i_L + i_L' \\ V_c + V_c' \end{bmatrix} = \begin{bmatrix} 0 & -\frac{(1-D-d')}{L} \\ \frac{(1-D-d')}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L + i_L' \\ V_c + V_c' \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} [V_g + V_g'] \quad (18)$$

$$[V_0 + V_0'] = [0 \quad 1] \begin{bmatrix} i_L + i_L' \\ V_c + V_c' \end{bmatrix} \quad (19)$$

In the above equations, the variables with superscript of dash represent the transient part and without dashrepresent the steady state part. Now the first right hand term of equation (18) can be splitted and rewritten as

$$\begin{bmatrix} 0 & -\frac{(1-D)}{L} \\ \frac{(1-D)}{C} & -\frac{1}{RC} \end{bmatrix} + \begin{bmatrix} 0 & -\frac{d'}{L} \\ \frac{d'}{C} & 0 \end{bmatrix} \left\{ \begin{bmatrix} i_L \\ V_c \end{bmatrix} + \begin{bmatrix} i_L{}' \\ V_c{}' \end{bmatrix} \right\} \quad (20)$$

By equating the steady state part to zero, the above expression can be reduced to the following including duty cycle in the input vector

$$\begin{bmatrix} \frac{1}{L} & \frac{V_0}{L} \\ 0 & -\frac{i_L}{C} \end{bmatrix} \begin{bmatrix} V_g \\ d' \end{bmatrix} \quad (21)$$

Now, the state equation for the small signal model of the boost converter can be written as

$$A = \begin{bmatrix} 0 & -\frac{(1-D)}{L} \\ \frac{(1-D)}{C} & -\frac{1}{RC} \end{bmatrix} \quad (22)$$

$$B = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \quad (23)$$

$$C = \begin{bmatrix} 0 & 1 \end{bmatrix} \quad (24)$$

VI. MODULATION SCHEME

The Nearest Level Control (NLC) methodology is utilised for producing the switching pulses at the fundamental switching frequency. It generates reduced switching losses and quite simple to implement for prototyping[21,22,23]. It produces higher harmonics for lower levels of the output waveform.

The harmonic voltage in respect to the Fourier series is shown below:

$$V_0(t) = \sum_{n=1,3,5}^{\infty} \frac{4V_{dc}}{n\pi} \cos(n\theta_k) \sin(n\omega t) \quad (25)$$

$$THD = \sqrt{\frac{\sum_{p=3.57}^{\infty} V_h}{V_1}} = \sqrt{\left(\frac{Vrms}{V_1}\right)^2 - 1} \quad (26)$$

$$V_{rms} = \frac{2\sqrt{2V}}{\pi} x \sqrt{\sum_{p=odd}^{\infty} \left(\sum_{k=1}^{N_L} \frac{\cos p\theta_k}{p} \right)^2} \quad (27)$$

where p = 3, 5, 7…. and V_h provides the order in which the harmonics increases and V_{rms} is the rms value of the output voltage.

V_1 is the voltage at the fundamental frequency which is given by equation (6).

$$V_1 = \frac{2\sqrt{2V}}{\pi} \times \left(\sum_{k=1}^{N_l} \frac{\cos p\theta_k}{p} \right) \quad (28)$$

$$\theta_k = \sin^{-1}\left(\frac{k-0.5}{N_l}\right), \quad k=1,2,3,\ldots\ldots N_l \quad (29)$$

The values of $\theta_1, \theta_2 \ldots\ldots \theta_{NL}$ are the switching angles which are calculated by using equation (29)

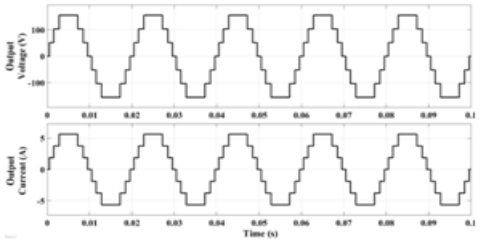

Fig. 10 Simulation results for R Load

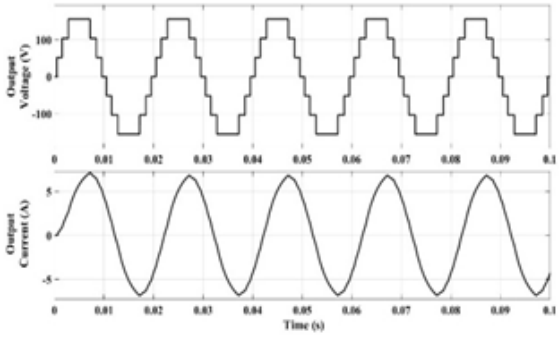

Fig. 11Simulation resultsfor RL Load

VII. SIMULATION RESULTS

The proposed topology is simulated on a R2015b MATLAB platform and voltages chosen are (V_1=100V, V_2= 200V). This produces seven levels at the output across a resistive inductive load of 80Ω and 100mH respectively. It uses NLM technique for producing switching pulses as it generates reduced switching losses. The simulation results ofoutput voltage and current are for R load are shown in Fig. 10. And both the parameters are in phase with each other. The FFT spectrum of the output voltage is shown in Fig.12 and %THD of output voltage is 10.1%.Thesimulation results of output voltage and current waveforms for RL load is shown in Fig.11 depicts theIt is seen here that the resistive inductive load acts like a low pass filter which generates a ripple free waveform of the output current.The %THD of output voltage and current which are illustrated in the Figs.13 and 14are 10.05% and 0.63%.

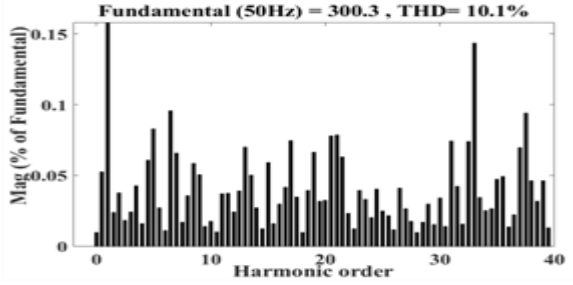

Fig. 12FFT spectrum for output voltage for R load

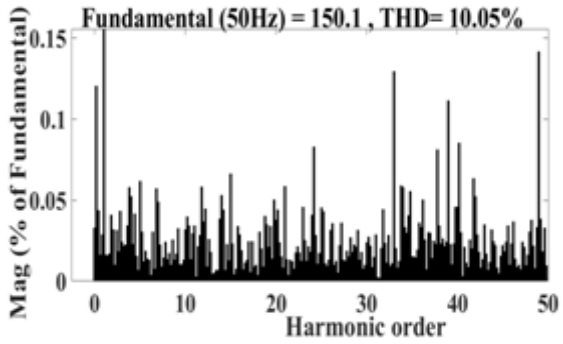

Fig. 13 Output voltage and current for RL load

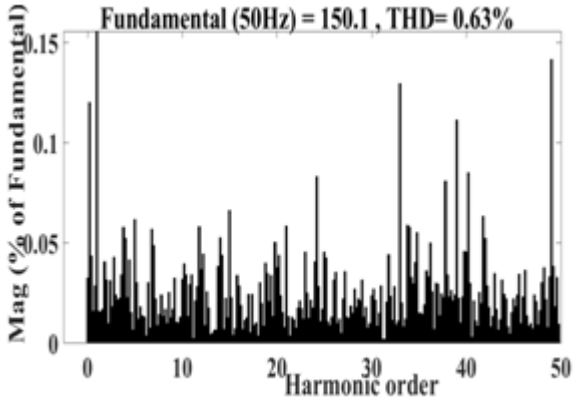

Fig. 14.FFT spectrum for output voltage for RL load

VIII. EXPERIMENTAL RESULTS

A prototype is fabricated in the laboratory. The NLM technique was utilised for generating the switching pulses by using the controller ATMEGA32P. The experiments results of output voltage and current for R load is shown in Fig.15.The RMS value of output voltage and current are 110.33V and 4.5A. The voltage THD of 11.3% is shown in Fig.16 .The hardware results for RL load is shown in Fig.17. The output current lags the output voltage because of the inductive nature of the load which acts like low pass filter. The RMS value of output voltage and current are 113.1V and 4.4A respectively. The values of voltage and current THD for RL load shown in Fig.18 and Fig.19 are 11.1% and 1.6% respectively. Thus, the experimental results are developed for resistive and inductive loads which are displayed in Table IV.

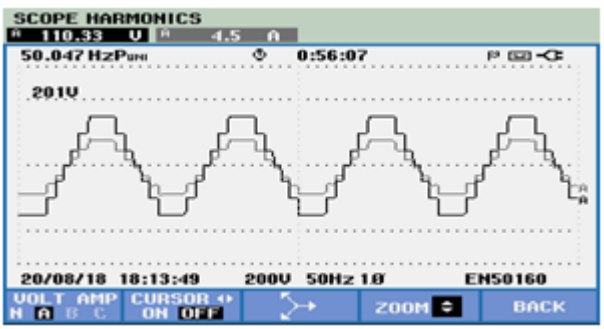

Fig. 15 Hardware results for R Load

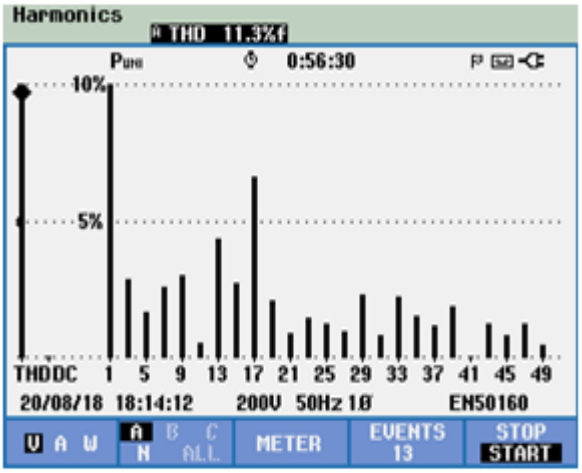

Fig. 16 Output Voltage spectrum for R Load

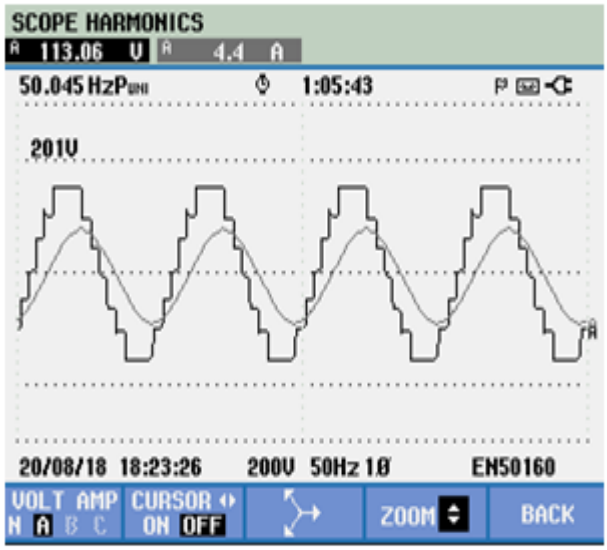

Fig. 17Hardware results for RL Load

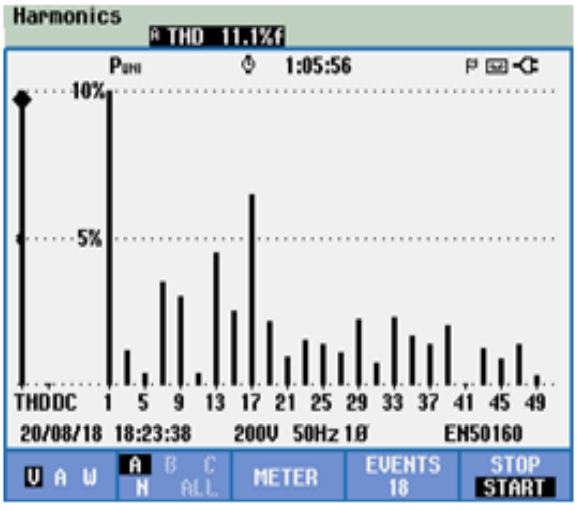

Fig. 18 Output Voltage spectrum for RL Load

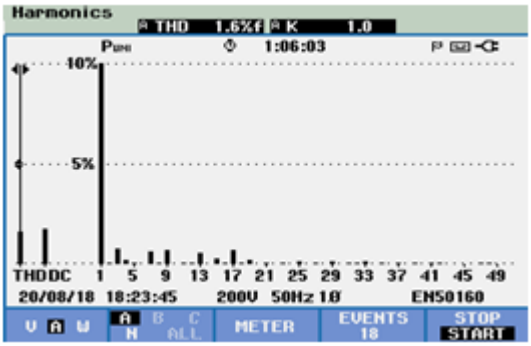

Fig. 19Output Current spectrum for RL Load

TableIII. Specifications of the Hardware Prototype

Parameters	**Values**
Output Voltage	110V
Output Current	4.5A
Switches	IRF640
Optoisolator	TLP250
Controller	ATMEGA32P
Resistance	50Ω
Inductance	32mH

Table IV. Experimental results for R and RL loads

Parameters	**Output Voltage(V)**	**Output Current(I)**	**THD$_V$ %**	**THD$_I$ %**
R load	110.33	4.5	11.3	11.3
RL Load	113.06	4.4	11.1	1.6

CONCLUSION

An asymmetrical MLI is implemented and P&O technique is utilized to maximize the power achieved through boost converter. The novelty of this structure lies in reducing the switch count and the requirement of DC sources. This also leads to the reduction of switching and conduction losses. The advantage of this topology is the ability to produce negative voltage levels without the addition of external H-bridge.The experimental results obtained confirms the feasibility of this topology.

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