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Design and Simulation of Thin Body Silicon Carbide MOSFET with Buried Oxide

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Abstract: ***Silicon carbide as a wide band gap semiconductor with attractive electrical and thermo physical properties has found its applications in high temperature, high power and radhard environment. However, silicon carbide MOS devices suffer from higher density of interface states than similarly oxidized silicon/SiO_2 interface. Improving the interface and electrical characteristics of silicon carbide MIS/MOS structure suitable for the above said applications is the current focus of the researcher. In this work, thin body silicon carbide MOSFET with buried oxide has been designed using TCAD and its electrical characteristics has been analyzed. Comparison of drain, transfer and capacitance voltage characteristics with conventional silicon carbide MOSFET reveals that thin body with buried oxide has improved the performance of MOSFET with higher gate capacitance, higher drive current and gain than conventional structure. Proposed SiC MOSFET with buried oxide exhibit higher gain with stable threshold voltage as the thickness of the body increases. Further, the proposed device exhibit higher field effect mobility than conventional MOSFET.***

Index Terms: ***Buried oxide; MOSFET; Silicon carbide; TCAD;***

I. INTRODUCTION

Functional temperature of semiconductor electronic devices is restricted to intrinsic temperature wherein concentration of intrinsic carrier exceeds intentionally introduced dopant impurities. Smaller band gap and associated high intrinsic carrier concentration results in restriction of intrinsic temperature of well developed silicon based electronic devices to 370ºC for a doping concentration of 10^{16} cm^{-3} [1]. This necessitates the move to semiconductors with larger band gap for high temperature applications. Incorporation of thicker and lightly doped drift region to increase the breakdown voltage (V_{BD}) of Si power devices results in higher on resistance (R_{on}) causing higher forward voltage drop. Hence there is a need for the use of semiconductor with high breakdown electric field in power devices which enable drift region thickness reduction while increasing the doping concentration for the same V_{BD} thereby maintaining the low on resistance (R_{on}) [2]. Further significant energy loss arising from the switching losses results in poor efficiency of the power converters of many silicon high power systems [3]. Since silicon semiconductor technology has approached it's theoretical limits in terms of operating temperature, breakdown voltage, switching frequency and efficiency, it becomes necessary to explore and study new semiconductor materials with superior properties for high temperature and high power applications. Wide band gap (WBG) semiconductors such as diamond, gallium nitride (GaN) and silicon carbide (SiC) are the possible candidates which could be used for solving the limitations imposed by the intrinsic properties of silicon in high temperature and high power applications. Larger band gap and associated low probability of thermal excitation of carriers form valence band to conduction band results in very low intrinsic carrier concentration which enables high temperature operations of WBG semiconductor. Ten times higher breakdown electric field of WBG semiconductors than Si enables ten times reduction in thickness of drift region and ten times increase in doping concentration this results in blocking region resistance (R_{on}) reduction hundred times for the given voltage rating which gives the benefit of smaller forward voltage drop of high power devices. High breakdown electric field of WBG semiconductor and associated thinner drift region enables much faster switching than silicon power devices with similar volt-amp rating. Higher switching frequency and the resulting smaller capacitors and inductors results in significant reduction of overall size and weight of the power converters made from WBG semiconductors which benefit both power and transportation industries [2]. Further high saturation velocity of WBG semiconductors allows power devices to switch faster than their Si counterpart [4].

Among the WBG semiconductors SiC is found to be the promising one with features such as known device process technology, commercial availability of quality substrate and the only compound semiconductor wherein oxide can be grown thermally in a similar fashion as that of Si. Being a WBG semiconductor the factors such as high temperature device processing, immature device fabrication technology and coefficient of thermal expansion mismatch with packaging material decimated the development of diamond semiconductor electronics for high temperature and high power applications [5]. Being a competitor to SiC with similar material properties, the drawback of GaN such as low thermal conductivity even lower than Si, non availability of GaN substrate and hard to achieve devices with higher power density give an edge to SiC over GaN. High thermal conductivity of SiC the value higher than that of copper enable effective transportation of heat from the power dissipated in the device [4]. Further high thermal conductivity results in less degradation of carrier velocity due to phonon scattering as it minimizes channel self heating [6]. According to NYSE the worldwide market for SiC and GaN power devices is projected to rise to \$3.7 billion in 2025 up from the current market value of just \$210 million.Majority carrier device and resulting high switching speed , simple gate drive, normally off characteristics and simpler topology makes MOSFET as a dominant switch than other switching devices such as IGBTs, BJTs, thyristors and JFETs [7].

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Further high input impedance and low switching loss of MOS structure results in more controllable power electronic circuits with higher efficiency than their BJT counterpart. Low packing density and higher power consumption approx. 2-3 times more power consumption of bipolar structure results in preference of MOS structure in storage applications [8].

It is found necessary to use a simulator tool to analyze the device characteristics prior to expensive real fabrication. Use of TCAD would help to reduce the cost and time required for the device development by up to 35-37% as estimated in International Technology Roadmap for Semiconductor (ITRS) 2012. TCAD simulation imitating the real fabrication process flow and characterization of semiconductor devices involves (i) virtual fabrication of the device either using process simulator or structure editor (ii) creation of mesh for device simulation (iii) solving the basic semiconductor equations which describe the behavior of the device and (iv) generation of figures and plots [9]. Process simulation mimics the manufacturing processes viz. oxidation, deposition, etching and thermal annealing is used to design real devices of different geometry. After process simulation the device is represented as a finite element meshes and each node of the device has its own associated properties such as material composition and doping density. Fine refinement of the grid are needed particularly near interfaces between different materials and regions of interest [10]. For each node, the microscopic quantities are computed by solving both the Poisson and carrier continuity equations numerically in a coupled manner using appropriate boundary conditions and the resulting macroscopic quantities such as electrical current, and voltage values of the device are plotted [11]. Selection of appropriate physical models viz. carrier transport mechanism, mobility models, velocity saturation, carrier generation and recombination, as well as quantum mechanical correction ensures realistic results from the device simulator.

II. Design and Simulation

In this work, two different MOS structures viz. conventional SiC MOSFET (D1) and SiC MOSFET with burried oxide (D2) have been designed using TCAD Sentaurus Sprocess and its electrical characteristics have been analyzed using device simulator Sdevice. Process simulation is initialized by specifying the SiC substrate type, dopant and doping concentration. 4H—SiC with Nitrogen doping concentration of 2×10^{15} cm^{-3} has been used as a substrate. Gate oxide was grown on SiC substrate using dry thermal oxidation performed at 1200° C for a duration of 10 min. The resulting gate oxide thickness is found to be 10 nm. Aluminum layer of 200 Å thick deposited on top of the dielectric material acting as a gate contact. MOSFET structure is obtained by anisotropic etching of both the gate metal and oxide using positive gate mask. Thickness in third dimension is assumed to be 1μm for 2D simulation of device. In order to obtain improved electrical characteristics, fine meshing is done in the gate oxide and gate oxide-SiC interface where the electric field is high compared to the bulk of the SiC and aluminum gate contact [12]. Before transferring the realized structure to the device simulator a new mesh is generated using mesh refinement that is optimized for better device simulation. In the case of D2, thin body SiC MOSFET is realized on a thick oxide layer deposited on SiC starting substrate. The resulting structures of both D1 and D2 are presented in Fig. 1 and Fig. 2 respectively.

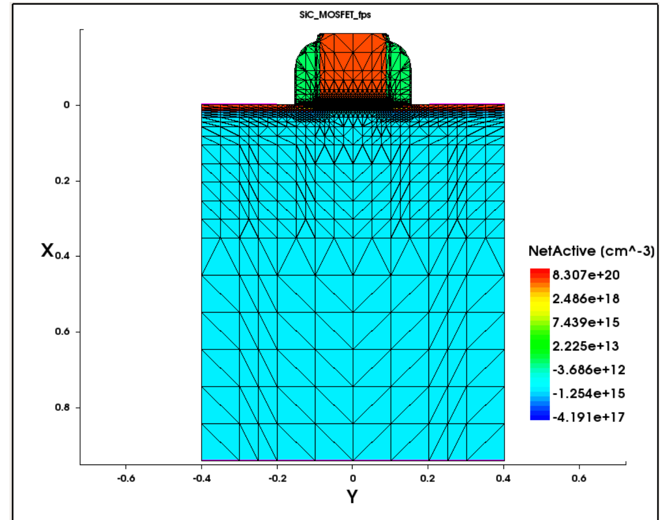

Fig. 1: Structure of conventional SiC MOSFET (D1)

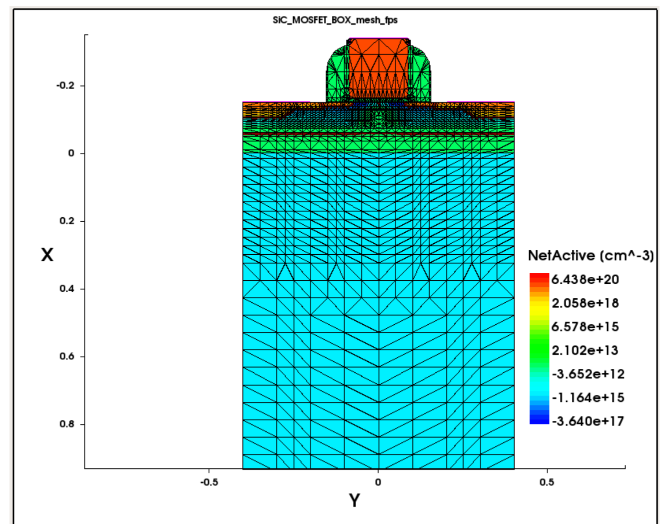

Fig. 2: Structure of SiC MOSFET with buried oxide (D2)

The Characteristics such as drain (I_d-V_{ds}), transfer (I_d-V_{gs}), capacitance voltage (C-V) and frequency dispersion of both structures are obtained using Sentaurus device simulator Sdevice. Device physics pertinent to SiC viz. incomplete ionization of dopant atoms, anisotropic mobility along different crystal axes are used along with velocity saturation, carrier generation recombination and quantum mechanical models during the simulation.

After defining the geometry of the device and physical models, five fundamental semiconductor equations describing carrier transport in the active region of the device were solved in a coupled manner using numerical solver. Gate capacitance of both the devices D1 and D2 were simulated by performing small signal ac analysis performed at a frequency of 1 MHz by sweeping the gate bias from 3 V to -2.0 V. Sentaurus svisual, the two dimensional plotting tool has been used for visualizing the simulated electrical characteristics.

III. RESULTS AND DISCUSSION

C-V characteristics presented in Fig. 3 exhibit deep depletion rather than inversion. This could be attributed to wide band gap and associated low intrinsic career concentration of SiC. It has been observed from the C-V characteristics that capacitance of MOSFET with buried oxide layer (D2) have slightly higher gate capacitance than those with conventional SiC MOSFET (D1). High gate capacitance results in high drain to source current for a given gate voltage. This could be observed from the drain characteristics given in Fig. 4. MOSFET with buried oxide exhibit better drain characteristics with higher drain current than conventional SiC MOSFET. Transfer (I_D-V_G) characteristics is obtained by sweeping the gate voltage in the positive direction for a constant drain voltage of 0.05 V. The resulting transfer characteristics is shown in Fig. 5. It has been observed that for the given gate to source voltage higher drain current is obtained in D2 when compared with those in D1. This implies that SiC MOSFET with buried oxide is capable of delivering higher gain than those with devices made from conventional SiC MOSFET. Since switching speed of the MOSFET is governed by both the output capacitance and the ability to source high current incorporation of buried oxide layer and resulting thin body SiC is found to improved the performance of SiC MOSFET.

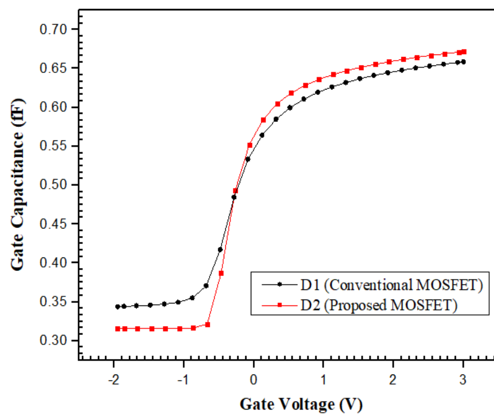

Fig. 3: Comparison of C-V characteristics of proposed MOSFET with conventional SiC MOSFET

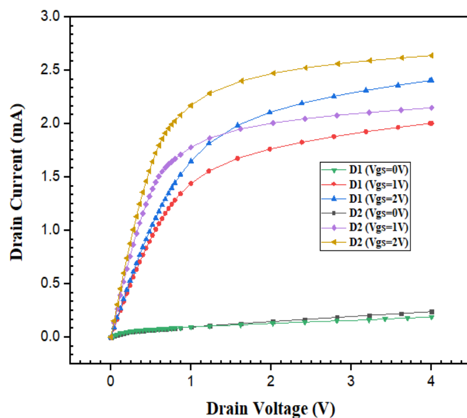

Fig. 4: Comparison of drain characteristics of proposed MOSFET with conventional SiC MOSFET

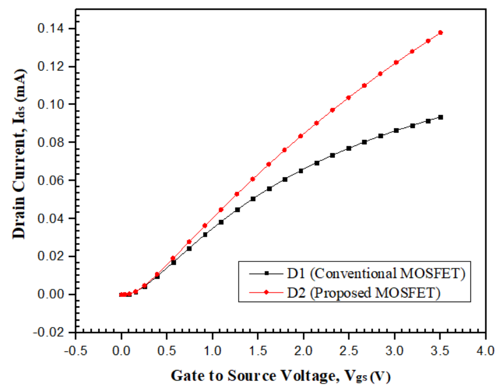

Fig. 5: Comparison of transfer characteristics of proposed MOSFET with conventional SiC MOSFET

Further, higher slope value of I_D-V_G characteristics of the proposed MOSFET results in higher field effect mobility (μ_{FE}) of proposed MOSFET structure [13]. This implies that field effect mobility is improved with buried oxide. In order to study the effect of frequency dispersion on the gate capacitance, C-V characteristics is simulated with different frequencies ranging from 10 GHz to 1 THz. It could be observed from Fig. 6 that C-V characteristics suffer from frequency dispersion in accumulation region in both the devices D1 and D2. Frequency dependent accumulation region could be attributed to the presence of surface charges [14].

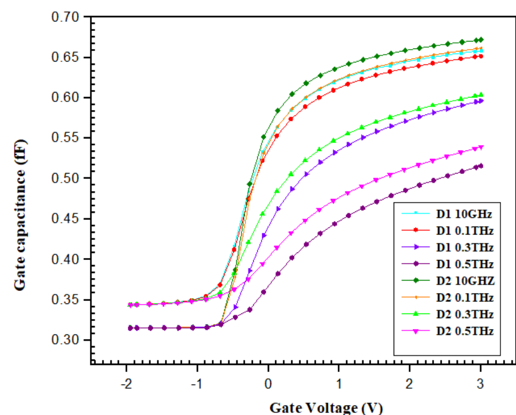

Fig. 6: Frequency dispersion characteristics of both proposed MOSFET (D2) and conventional MOSFET(D1)

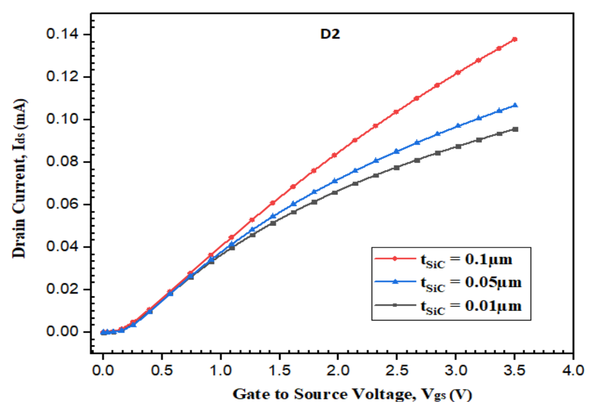

Fig. 7: Transfer characteristics of proposed MOSFET (D2) with different body thickness (t_{SiC})

Transfer characteristics of proposed MOSFET (D2) with different body thickness is studied and its results are given in Fig. 7. It could be observed that there is no significant change in threshold voltage with body thickness (t_{SiC}) which implies the threshold voltage stability of proposed MOSFET. As the threshold voltage is stable floating body effect could be reduced by reducing SiC body thickness. Further, higher drain current is obtained for the given gate to source voltage (V_{gs}) as the thickness of the body increases. This shows that increase in body thickness increases the gain of the MOSFET without degrading the threshold. Further increase in slope with thickness of the body implies that field effect mobility could be improved by increasing the thickness of the body.

IV. CONCLUSION

Thin body Silicon carbide MOSFET with buried oxide has been designed using TCAD process simulators and its electrical characteristics viz. drain, transfer and capacitance voltage were analyzed using device simulator. Analysis reveals that incorporation of buried oxide with thin body results in improved performance with higher capacitance, higher drive current and higher gain. Further MOSFET with buried oxide structure exhibit threshold voltage stability with higher gain as the thickness of the body increases. Field effect mobility is improved with proposed structure compared to conventional MOSFET. Further improvement in field effect mobility is achieved by increasing the thickness of body.

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