A 2.2 V-Voltage Reference Circuit Design with TC of 35.49 ppm/°C for low power DAC Applications

Chaithanya Mannepalli, Sreenivasa Rao Ijjada, Rajesh Kumar Srivastava

Abstract— Constant voltage reference is the basic for the digital data conversion from analog data where rich digital data applications are important. It acts as a bench mark reference for the data to convert. In this paper we have designed a BGR supplying 1.4 V using 5 V supply and generated a constant supply of 2.2 V with additional ciruit using SCL 180 nm technology where the TC is 35.49ppm/oC and the mean and SD of Monte carlo resulted as 74.81 and 11.09 respectively, which can be used as a benchmark reference for DACs.

Keywords- Voltage reference, process voltage and temperature(PVT), temparature coefficent(TC), Standard deviation(SD)

I. INTRODUCTION:

Shrinking device dimensions in advancing CMOS technologies require accurate supply voltages to ensure device reliability. As a result, analog circuit designers are faced with many challenges in finding new ways to build analog circuits that can provide accurate supply voltages while maintaining performance. As reference voltages, their accuracy plays a vitally important role in determining the performance of subsequent circuits. For example, BGR circuits are utilized in analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), which require high-accuracy reference voltages to provide high-resolution and high speed data conversion. Some BGRs with low supply voltage are reported by using low threshold device [1], [2], Bipolar process [3], Bi-CMOS process [4], DTMOS process [5], which are either expensive or difficult to be integrated with digital system. This has resulted in the development of CMOS curvature-corrected BGRs in low supply voltage, such as piecewise-linear [6] and piecewise nonlinear curvature correction [7], temperature-dependent resistor ratio [8], current subtraction of two BGRs [9]. In this work we have designed a basic BGR and tried to multiply the voltage with an additional circuitry such that it supplies a constant 2.2 V for the DACs.

II. ARCHITECTURE AND DESIGN ANALYSIS

In this we have designed a constant voltage reference circuit with the use of operational amplifier which is connected in negative feedback as shown in fig.1 and the

Revised Manuscript Received on April 12, 2019.

node voltages at the inputs of operational amplifier will generate PTAT voltage which is copied to the M3 transistor using current mirror and Q3 will be generating the CTAT which is then added to PTAT for generating reference voltage. Resistors R1 and R2 are used to adjust the behaviour of voltage reference curve. Since the designed circuit is self-biased basic BGR circuit may lead to the startup issue which pushes the circuit into off state such for this we have designed a start-up circuit which helps to maintain the functionality of the circuit. For start-up M4, M5, M6, M7 and resistor R3 is used.

Constant 2.2 V voltage reference circuit using BGR is shown in fig.2 where the designed BGR provides the voltage to the OpAmp which can be adjusted by successfully adjusting resistors R1 and R2 from equation 1, A PMOS transistor is attached in the final stage such that the constant Vref is not dependent on the Vdd.



Fig.1. Constant voltage reference with start-up circuit



Fig.2.Constant 2.2 V voltage reference circuit using BGR

Published By: Blue Eyes Intelligence Engineering & Sciences Publication



Retrieval Number: F12690486S419/19©BEIESP DOI: 10.35940/ijitee.F1269.0486S419

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$$V_{ref} = \frac{R1 + R2}{R1} (V_{BGR})$$
(1)

III. **RESULTS AND ANALYSIS**

BGR with start-up is designed using SCL 180nm Technology library in cadence virtuoso and the results are analysed. Basic BGR using Operational Amplifier output is shown in fig.3. Output curve of voltage reference is shown in fig.5 for baic BGR with start-up voltage ranging from 1.433 to 1.448V for temperature range of -40 to 125°C and at 27°C generated 1.448 V with a TC of 48.84 ppm/°C. The montecarlo analysis of the basic BGR with start-up is shown in fig.4 for 200 samples and the mean and standard deviation of Temperature coefficient (TC) is 66.5007 and 7.42 ppm/°C respectively.



Fig.3. Output of BGR with start-up



Fig.4.Monte Carlo Analysis for TC of BGR with startup



Fig.5. Output of Constant 2.2 V voltage reference using **BGR at 45 corners**

Constant 2.2 V voltage references using BGR is designed using SCL 180nm Technology library in cadence virtuoso and the results are analysed. Where 45 corner output is shown in fig.5 which doesn't show much variation.Output curve of voltage reference is shown in fig.5provides a voltage around 2.2 V of -40 to 125°C and at 27°C generated 2.24 V with a TC of 48.84 ppm/ $^{\circ}$ C.



Fig.6. Monte Carlo Analysis for TC of Constant 2.2 V voltage reference using BGR at 45 corners



Fig.7. Monte Carlo Analysis for Vref of Constant 2.2 V voltage reference using BGR at 45 corners

The montecarlo analysis of the Constant 2.2 V voltage reference using BGR is shown in fig.6 and fig.7 for 200 samples and the mean and standard deviation of Temperature coefficient (TC), voltage refenece is 74.811 and 11.09 ppm/°C,2.226 V and 0.38V respectively.

Table.1. shows the comparison between the designed constant 2.2 V voltage reference using BGR, BGR with startup and the other published state- of- the-art reference circuits. The Standard deviation for the BGR with startup is less than the Basic BGR and the TC of BGR with start-up also showed a nominal change of 7.42 ppm/°C.The constant 2.2 V voltage reference using BGR work at 5 V supply using 0.18 µm technology at a temperature range of -40 to 125 °C which is greater than other circuits and shown a TC of 35.49 ppm/°C which is less when compared to other circuits in the table.



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	Supply	Technology	TR	TC	М-	SD-	Vref	M-Vref	SD- Vref
					TC	ТС			
[10-2013]	1.8V	0.18 µm	-40 to 120	147	-	-	1.09	1.05	3.68m
[11-2015]	1.15V	90nm	0 to 100	53.1	45.1	-	720m	730m	6.3m
[12-2017]	3.3V	0.35 µm	0 to 110	105	136.5	44	-	-	-
BGR with	5V	0.18 µm	-40 to 125	48.84	66.5	7.42	1.448	1.524	0.18
Startup[This Work-									
2019]									
Constant 2.2 V	5 V	0.18 µm	-40 to 125	35.49	74.81	11.09	2.198	2.226	0.38
voltage reference									
using BGR									

Table.1. Comparision of Basic BGR and Basic BGR with startup

TC: Temperature Coefficient (ppm/°C)

M-TC: Mean of Temperature Coefficient (ppm/°C)

SD-TC: Standard deviation of Temperature CoefficientVref: Reference Voltage (V)

M-Vref: Mean of Reference Voltage (V)

SD- Vref: Standard deviation of Reference Voltage

TR- Temperature Range (°C)

IV. CONCLUSIONS

BGR with start-up is designed at 5 V supply providing a reference voltage of 1.448 V using SCL 0.18µm technology and this BGR is used to provide voltage for the proposed circuit whih helps in generation of constant 2.2 V voltage reference uing BGR. Both the designs are tested for montecarlo analysis for 200 samples. The reults, BGR with startup showed the TC at 27°C as 48.84 ppm/°C .Whereas TC at 27°C for constant 2.2 V voltage reference using BGR is 35.49 ppm/°C. Inspite of increse in the constant voltage refrence value from 1.448 V to 2.2 V we obtained a lower TC at 27°C.

REFERENCES:

- G. Giustolisi, "A low-voltage low-power voltage reference 1. based on subthreshold MOSFETs," IEEE J. Solid-State Circuits, vol. 38, no. 1, pp. 151-154, Jan. 2003.
- H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, 2. S. Atsumi, and K. Sakui, "A CMOS bandgap voltage reference circuit with sub-1-V operation," IEEE J. Solid-State Circuits, vol. 34, no. 5, pp. 670-674, May 1999.
- 3. M. Gunawan, G. C. M. Meijer, J. Fonderie, and J. H. Huijsing, "A curvature-corrected low-voltage bandgap reference," IEEE J Solid-State Circuits, vol. 28, no. 6, pp. 667-670, Jun. 1993.
- 4. P.Malcovati, F.Maloberti, M.Pruzzi, and C.Fiocchi, "Curvatur ecompensated BiCMOSbandgap with 1-V supply voltage,' IEEE J SolidState Circuits, vol. 36, no. 7, pp. 1078-1081, Jul. 2001.
- 5 A.-J. Annema, "Low-power bandgap voltage references DTMOSTs,"IEEEJ.Solidfeaturing StateCircuits, vol.34, no.7, pp.949-955, Jul. 1999.
- G. A. Rincon-Mora and P. E. Allen, "A 1.1-V current-6. mode and piecewise-linear curvature-corrected bandgap reference," IEEE J. Solid-State Circuits, vol. 33, no. 10, pp. 1551-1554, Oct. 1998.
- J. H. Lee, Y. N. Fu, and Y. S. Wang, "A 1-V piecewise 7. curvaturecorrected CMOS bandgap reference," in Proc. IEEE Int. Symp. Low Power Electron.Des., Bangalore, India, 2008, pp. 289–294.
- K. N. Leung and P. K. T. Mok, "A 2-V 23 A 5.3 ppm/ 8. curvaturecompensated CMOS bandgap voltage reference," IEEE J. Solid-State Circuits, vol. 38, no. 3, pp. 561-564, Mar. 2003.

- M. D. Ker and J. S. Chen, "New curvature compensated 9. technique for CMOS bandgap reference with sub-1-V operation," IEEE Trans. CircuitsSyst.II,AnalogDigit.SignalProcess.,vol.53,no.8,pp. 667-671, Aug. 2006.
- Yuji Osaki, Tetsuya Hirose, Nobutaka Kuroki and 10. Masahiro Numa "1.2V Supply, 100nW,1.09-V Bandgap and 0.7-V Supply, 52.5 nW, 0.55-V Subbandgap Reference circuits for Nanowatt CMOS LSIs ," IEEE J. Solid-State Circuits, vol. 48, no. 6, pp. 2180-2186, Jun. 2013.
- 11. Kin Keung Lee, Tor SverreLande and Philipp DominikHafliger "A Sub-µW BandgapRefere Circuit with an inherent curvature compensation property," IEEE Transactions on Circuits and Systems-I, vol. 62, no. 1, pp. 1-9, Jan. 2015.
- 12. DimitryOsipov and Steffen Paul , "Temperaturecompensated β-Multiplier Current reference circuit," IEEE Transactions on Circuits and Systems-II, vol. 64, no. 10, pp. 1162-1166, Oct. 2017.



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