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Multi-Level Memristor Memory: Design and Performance Analysis

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Abstract*: Memristor-based memories are one of the attractive candidates to replace present memory technologies due to its novel characteristics such as non-volatile storage, nanosize cell, compatibility with CMOS, low power dissipation, and multi-level cell (MLC) operation etc. However, the device needs to overcome the potential challenges such as process variations, non-deterministic nature of the operation, sneak path issues, non-destructive write and read operation. One of the most important characteristics of memristor memories is its ability to store multiple bits in one cell. In this paper, we design a low power, high-speed multi-level memristor based memories. Additionally, the performance analysis of the multi-level memristor memories has been performed under various memristor models and window functions.

***Index Terms*: Memristor, Non-volatile memory,**

I. INTRODUCTION

Ever since the theoretical prediction of a memristor in 1971 by Chua[1] and its experimental identification in 2008 by HP Laboratories[2], the newly introduced electrical component has gained a lot of attention by many research groups. The continued migration of technology into deeper and smaller scales of measurement has led to several hybrid nanodevices and methodology to replace the existing CMOS technology and have a low power consumption with no/less performance degradation with an increasing requirement for higher and more compact storage of data and reducing the effective cost and increasing density. The memristor is a nanoscale device capable of performing demanding needs. The theoretical design of the memristor was based on the concept of symmetry between mathematical definitions of three basic passive components, i.e. resistor, inductor, capacitor and four basic circuit variables i.e. current, flux, charge and voltage. The basic relationship between the passive element and the circuit variables include: $R = dv / di;$ $C = dq / dv; L = d\varphi / di$ and within the circuit variables: $i = dq / dt$; $v = d\varphi / dt$. Out of the six one-to-one relationships between the stated four circuit variables, five were well defined. To address the missing sixth relationship Chua stated a missing passive element to the already existing three and named it the memristor. The memristor was defined as $M = d\varphi / dq$. The memristor has many applications, including memory elements, analog to digital converters[3], neural-fuzzy networks, chaotic circuits, logic and processing devices. The memristor as memory devices is one important and attention seeking application and this has made it very special in the field of VLSI. The memristor can switch from one state to another depending on the current or voltage values. This switching property can be defined by using a two terminal device i.e. memristor rather that a three-terminal transistor. By varying the device resistance between a low and high value, depending on various internal parameters of the memristor device and also the fabrication process and parameters, the data can be stored. The memristor is an alternative candidate for SRAM cells. In SRAM[4–6], the data is stored in the form of voltage but in the case of a memristor, the data is stored in the form of resistance. Many logical operations can be carried out by the device and hence in-memory calculation can also be performed.

The memristor acts as a memory cell, as it has a special property of storing the previous state. It stores the previous state depending on the resistance property of the device. By varying the resistance property we can obtain any value ranging from the low state to high state. The memristor memory device is a non-volatile storage memory. Even if the external stimulus is removed the data is stored for over a decade. This property of a single memristor can be used in designing a memory cell to store data.

In this paper, we propose methods to write and read multiple data in a single memristor with sufficient noise margins and without much external circuitry. The storage of data in a single memristor using the multi-level structure[7] can enhance the overall data density on the storage device. Also, an analysis was drawn between the various models and window functions available along with a comparison between the switching speeds and power consumptions in each case. Also, we have also implemented multi-level[7] write operation using the crossbar array architecture with memristors using Voltage threshold adaptive memristor (VTEAM)[8]. We have focused on two models and applied various window functions to obtain switching speeds and power.

II. MEMRISTOR MEMORY: OPERATION AND MODELING

A. Memristor operation

Resistive random access memory, also called the memristor, is a two-terminal non-volatile memory device where the switching medium, metal oxide, is sandwiched between two electrodes. The memristor stores information by varying the resistance of the cell. The memristive devices have a distinguishable pinched hysteresis loop in the first and third quadrants of the V-I plane [8].

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Much, like the phase change memory, a low resistance state (LRS) or ON state is used to represent logic "1" and a high resistance state (HRS) or OFF state is used to represent a logic "0". To switch the ReRAM cell between the two states an external voltage needs to be applied to the metal oxide layer. The switching from LRS to HRS is called RESET operation and the switching from HRS to LRS is called SET operation. In such designs, the power consumption and switching time are parameters of utmost importance and need to be analyzed.

There are basically two switching modes in the metal oxide ReRAM – (i) unipolar mode: The direction of switching depends only on the amplitude of the external voltage applied and not on the polarity of the voltage applied. Thus, set/reset can occur at the same polarity. (ii) Bipolar mode: The direction of switching depends on the polarity of the voltage applied. Hence, RESET occurs at one polarity and SET occurs at the opposite polarity[9]. The major advantage of memristive devices compared to other memory devices is that they have a high density and retain memory.

B. Memristor Models

i. Linear Ion drift model:

This model[10] can be represented as a series combination of two resistors, one resistor representing high conductance and the other resistor representing low conductance. This model assumes that vacancies are free to move throughout the entire device length with the ions having the same average ion mobility in a uniform field. This model exhibits the hysteresis characteristic of memristors, but it is inaccurate as it has certain limitations[11],[12].

ii. Nonlinear ion drift model

In this model, the memristor is assumed to be a voltage-controlled device with a non-linear dependence between the state variable and voltage[13]. This model assumes an asymmetric switching behavior and the state variable w is normalized between the interval [0, 1].

iii. Simmons tunneling barrier model

This model[14] has a resistor in series with an electron tunnel barrier. Due to the exponential dependence of the ionized dopants this model assumes an asymmetric switching and non-linear behavior. This model is more accurate and the Simmons tunnel barrier has a width represented by state variable w.

iv. ThrEshold Adaptive Memristor model (TEAM)

This is a very generic and simple model[14] which fits all the previously mentioned models with a small error which is acceptable. This model assumes (i) below a certain threshold there is no change in the state variable. (ii) a dependence in polynomial level exists between the derivative of the internal state drift and the memristor current. In this model, the simulation runtime is boosted by 47.5% and is computationally more efficient [11].

Voltage ThrEshold Adaptive Memristor model (VTEAM)

This model[8] as proposed by Kvatinsky, has better accuracy (below 1.5% in terms of relative RMS error). This model comes with the advantages of the TEAM model like generality, accuracy, and flexibility. As the state variable w moves towards the boundary Woff, the resistance increases in the VTEAM model. This model exhibits a threshold voltage. By tuning the fitting parameters, sufficient accuracy to the experimental data can be achieved by the VTEAM model.

III. MEMRISTOR MEMORY: WINDOW FUNCTIONS

For each model of the memristor, the state variable (w (t)) operates within a certain boundary. To limit the specific state variable within its range and to bring in practical non-linear characteristics and asymmetry at the boundaries, the state variable and the window functions are multiplied.

i. Joglekar window

The Joglekar window proposed by Joglekar[15] and wolf in 2009, Is a generic symmetric window function, whose non-linearity is controlled by p (control parameter).
Window function of Joglekar window:

$$F(x)=1-(2x-1)^{2p} \qquad (x=w/D) \qquad (1)$$

Just like a rectangular window function, with the increase in control parameter p the non-linear drift phenomenon decreases. The maximum value is reached at the center (w=D/2) and reaches 0 towards the boundary. In the Joglekar window, when the state variable w achieves w=0 or w=D (extreme values), the window function value becomes 0. Therefore when the memristor is either at its LHS or RHS it is impossible to change its state even after the application of an external stimulus.

ii. Biolek window:

The Biolek window[13] in 2009 was proposed to render the inaccuracy of the Joglekar window function, i.e. the state variable at the terminals cannot be changed by an external stimulus (stuck at the boundary). Window function of Biolek window:

$$F(x)=1(x-\mathrm{sgn}(-i))^{2p} \quad \begin{cases} \mathrm{sgn}(-i)=1, \text{ when } i>=0 \\ \mathrm{sgn}(-i)=0, \text{ when } i<0 \end{cases} \qquad (2)$$

The Biolek window, the fact that the speeds of approaching and leaving the boundary of the limits are different. This window function depends on the input current I (current controlled memristor).

The Biolek window function is a multivariate function which makes it difficult for analysis. Also at the boundaries, there is no continuity condition.

iii. Prodromakis window:

The Prodromakis window[15] was proposed to overcome the problems of the previous Biolek window, i.e. there is no continuity condition at the boundary and also not scalable and cannot be adjusted. The maximum value of the Biolek function is only one and cannot be lower or higher.
Window function of Prodromakis window:

$$F(w)=j(1-[(w-0.5)^2+0.75]^P) \qquad (3)$$

A control parameter j, specifies the highest value of the function, which can be lesser or greater that one.

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iv. Kvatinsky window:

The proposed Kvatinsky window[16] is used to fit the Simmons tunnel barrier model. This window has two window functions, one for ON switching and one for OFF switching.

$$f_{HRS}(x) = \exp\left(-\exp\left(\frac{x - x_{HRS}}{w_c}\right)\right) \quad (4)$$

$$f_{LRS}(x) = \exp\left(-\exp\left(\frac{x_{LRS} - x}{w_c}\right)\right) \quad (5)$$

X_{HRS}
and X_{LRS} are positive parameters and R_{HRS} and
R_{LRS} are effective resistances at the bounds respectively.

IV. MEMRISTOR MULTILEVEL CELL

Resistive Random Access Memory (ReRAM) are two-terminal devices in which the switching medium is placed between the top and bottom electrodes. The resistance of the switching medium can be controlled by applying the required current or voltage. Memristor shows resistive switching behavior as it has a metal-insulator-metal configuration, the insulator operates as the storage medium. The basic physical memristor equation is $d\Psi = M.\ dq$

Where $d\Psi$ and dq are infinitesimal values of magnetic flux and electric charge respectively. M is the memristance of the device as a function of electric charge. The memristor can be modeled as two series resistors, which was introduced by HP laboratories. The two variable resistors in the series determine the total resistance of the device.

The insulator film has two regions, one with a high concentration of dopants, has low resistance RON and the other region having a low concentration of dopant and much higher resistance ROFF as shown in Fig1. Applying a negative voltage at the terminals of the memristor varies the resistance from low (RON) resistive state to high (ROFF) resistive state and if a positive voltage is applied to the memristor the vice versa takes places. The memristor can be defined as a function of the state variable w and is related to the length D.

$$M(w) = R_{ON} \times \frac{w}{D} + R_{OFF}\left(1 - \frac{w}{D}\right)$$

$$\text{where } 0 \leq \frac{w}{D} \leq 1 \quad (6)$$

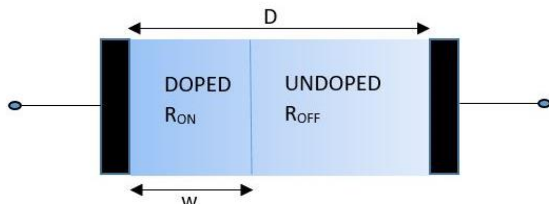

Fig1. The physical model of a memristor model.

In fig1. RON is the lowest resistance possible and ROFF is the highest resistance possible for a given memristor. The total length of the device is D, usually in nanometres. w is the state variable of the memristor, it is defined as the imaginary boundary between the doped and undoped region as in fig1.

As mentioned by Strukov et al. in his paper, the value of the state variable w is determined using the equation.

$$\frac{dw(t)}{dt} = \mu(v) \times \frac{R(on)}{D} \ .\ q(t)\ .\ F(w,D) \quad (7)$$

μV is the average dopant mobility in the memristor and F(w,D) is the window function. The boundary limits are maintained using the window function.

A voltage pulse of sufficient width and amplitude higher than the threshold is applied to memristor to store data. We have devised two methods to write and store data into the memristor, i) Keeping the pulse width constant and varying the amplitude and ii) keeping the amplitude constant and varying the pulse width of the voltage to store multi-level data onto a single memristor[7]. To store multiple data into the memristor we can use Vdd as maximum voltage and -VCC as the lowest level, which store two levels and the intermediate levels between Vdd and -VCC can be used to store multiple levels. This methodology can be used for both read and write operations.

The length of the memristor D is divided among four states with widths w1, w2, w3, w4. Data can be stored within these widths using the required voltage or current and a sufficient noise margin between each is provided. We can have a uniform margin memristor device in which the widths (blue shaded) and noise margins (black shade) are equal. The noise margins must be adequate between adjacent states. Writing data to each region depends on the characteristics of a memristor, fabrication technology, pulse width and the amplitude of voltage input. The number of memory levels can be increased to store more than quaternary data. This reduces the noise margins and as the number of levels increases, the complexity of storage also increases. In this paper, we have used non-uniform margins for quaternary data storage. The width and the noise margins distance are not uniform as seen if fig.2.

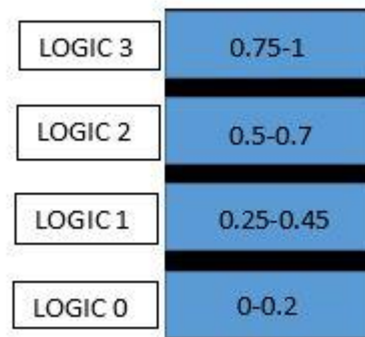

Fig.2. Memristor divided into four regions for Quaternary date storage having non-uniform width margins.

A. Write operation

Memristors can switch between a low resistance state and high resistance state and hence store two logic states. For the memristor to store more than two logic states the number of resistance levels needs to be increased.

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By switching between these quantized resistances levels, multiple logic levels can be stored in a single memristor cell. In this paper, we have used two methods to achieve these multiple levels.

The first method is by varying the input pulse amplitude keeping the pulse width constant[17]. The state (width position) of the memristor changes in accordance with the amplitude of the applied voltage. Thus, we are able to store D1, D2, D3, and D4 at different states by varying the amplitude of the input voltage which is proportional to the data to be stored as shown in Table 1.0 for VTEAM model and in Table 1.1 for linear ion drift model. Fig.3 shows the MLC implementation using the VTEAM model while varying amplitude whereas Fig.4 shows MLC implementation using a linear ion drift model while varying amplitude

Table1.0.shows the four levels in which data can be stored by varying amplitude of voltage to achieve the four states for the VTEAM model.

	Normalized Width Position	Voltage (V)
D1	0-0.2	0.2
D2	0.25-0.45	0.75
D3	0.5-0.7	1.15
D4	0.75-1	1.6

Table1.1.shows the four levels in which data can be stored by varying amplitude of voltage to achieve the four states for the linear ion drift model.

	Normalized Width Position	Voltage (V)
D1	0-0.2	0.6
D2	0.25-0.45	1
D3	0.5-0.7	1.33
D4	0.75-1	1.6

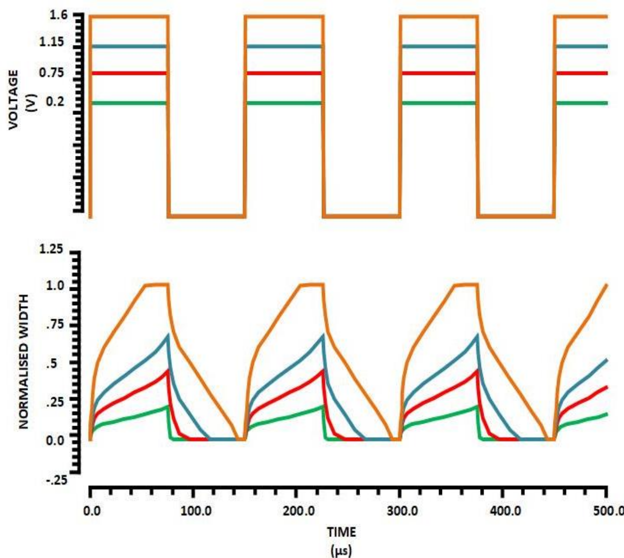

Fig.3 MLC implementation using the VTEAM model while varying amplitude

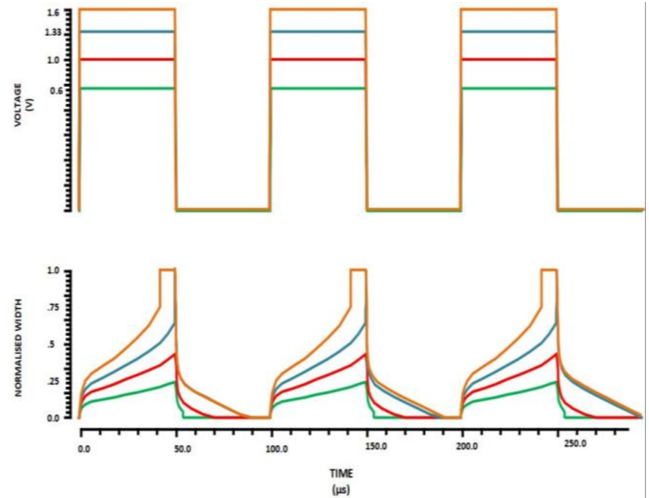

Fig.4 MLC implementation using a linear ion drift model while varying amplitude

The second method is by varying the pulse width keeping the amplitude of the input voltage constant. The state (width position) of the memristor increases on the pulse width of the input pulse increases. Hence we are able to store D1, D2, D3, D4 at four different levels as shown in Table 2.0 for the VTEAM model and in Table 2.1 for the linear ion drift model. Fig.5 shows MLC implementation using the linear ion drift model while varying pulse width whereas Fig.6 shows MLC implementation using the linear ion drift model while varying amplitude. Fig.7 shows the MLC implementation using the VTEAM model while varying the negative amplitude.

Table2.0 shows the four levels in which data can be stored by the varying pulse width and the number of pulses to achieve the four states for the VTEAM model.

	Normalized Width Position	No. of pulses	Voltage (V)
D1	0-0.2	1	0.22
D2	0.25-0.45	2	0.43
D3	0.5-0.7	3	0.65
D4	0.75-1	4	0.85

Table2.1 shows the four levels in which data can be stored by the varying pulse width of voltage to achieve the four states for the linear ion drift model.

	Normalized Width Position	Pulse Width (nm)
D1	0-0.2	30
D2	0.25-0.45	107
D3	0.5-0.7	170
D4	0.75-1	220

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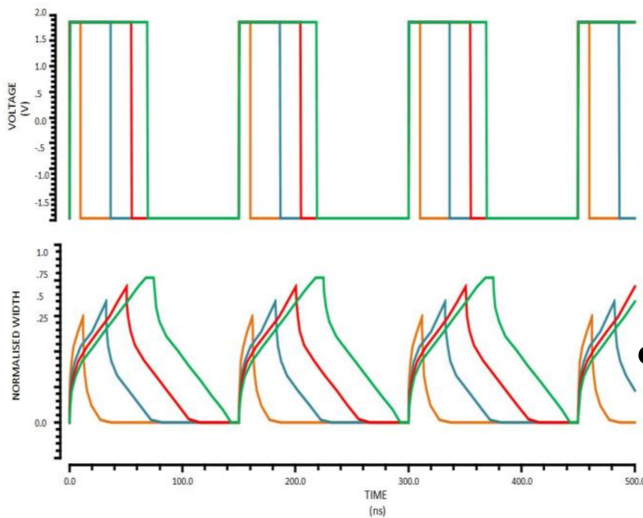

Fig.5 MLC implementation using the VTEAM model while varying the pulse width

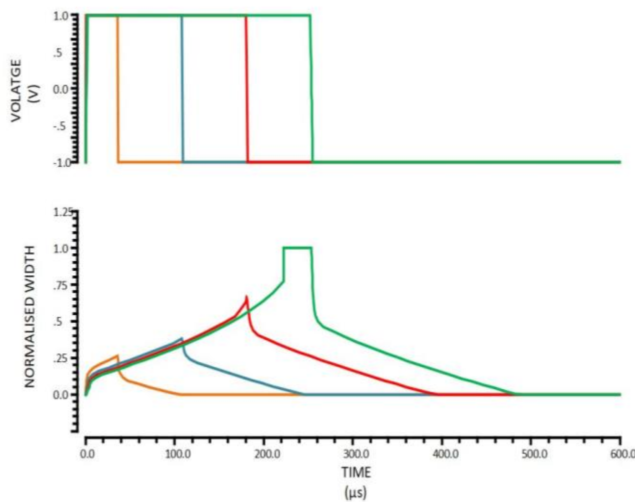

Fig.6 MLC implementation using a linear ion drift model while varying amplitude

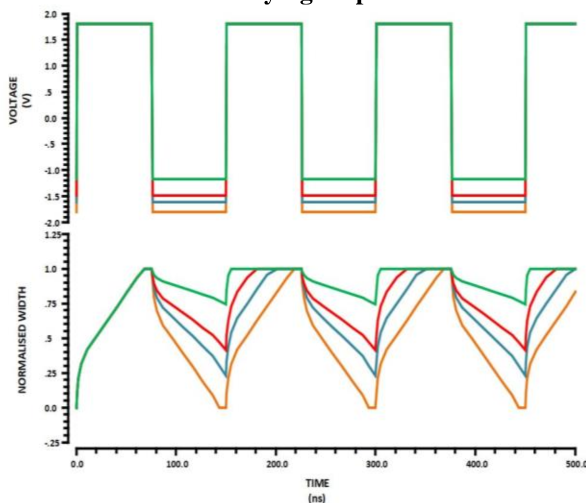

Fig.7 MLC implementation using the VTEAM model while varying the negative amplitude

B. Read operation

Reading multi-level data from a single memristor is more challenging than the write operation[18],[19]. As a single device stores different levels of the resistance, to read the data a stimulus is applied across the memristor, the stimuli can be a voltage pulse. Corresponding to the state of the memristor an output is generated and the data can be read. But after consecutive read operations, the resistance and the state variable w get altered and may produce an incorrect reading. To overcome this issue, after each read operation, we apply another pulse with opposite polarity[20] to the initial pulse, to bring the memristor back to its initial state. As the memristor is based on charge and magnetic flux relationship and not on voltage or current, the waveform of the error correcting pulse is not uniform or important. As long as the later waveform provides the same charge or flux to revert the error due to the read operation.

C. C. Crossbar MLC operation

Simulations were performed on a crossbar of size 4x4 consisting of 16 memristors as shown in Fig.8. This structure can be extended for 16x16 crossbar as well as other larger crossbar memristor circuits.

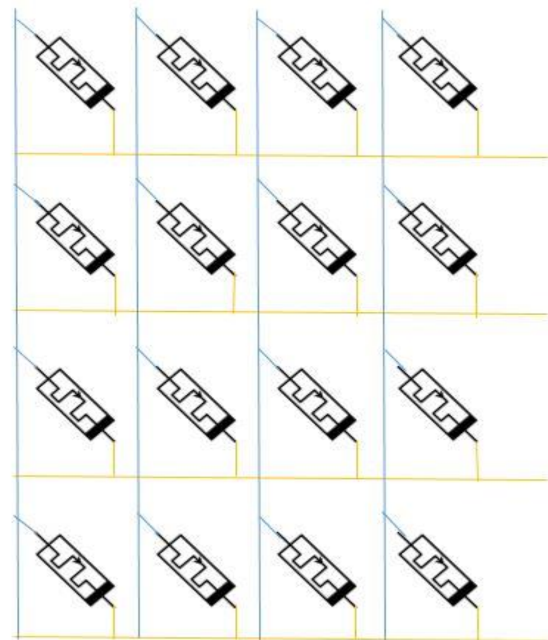

Fig. 8 Crossbar of size 4x4 consisting of 16 memristors

In this design all the cells are interconnected forming a dense grid, eliminating the access transistors to achieve the smallest theoretical size of $4F^2$. This results in a maximized area efficiency of the array. A voltage of $-V_W$ (-1.8V) is applied to the selected row and all other rows are grounded. A voltage of V_w is applied to the column where 1 has to be written and all other columns are set at $-V_W$. This process will result in writing 1 in the selected memristor cell. This selection process can be achieved with the help of row and column decoders. We also observed degradation in the signal across unselected memristors due to sneak path currents. Even if the voltage across the cell is below the threshold voltage, the cells conduct small amounts of current and exhibit nonideal behavior. Ideally, the cells with the insufficient voltage across them do not conduct. But in practice, a sneak path current is observed. This degradation increases as the size of the memristor crossbar increases.

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V. SIMULATION RESULTS AND ANALYSIS

A. Memristor switching time

Switching in a memristor[19] always takes place with a time delay. An electron always possesses a certain amount of inertia. The flux φ or the charge q has the tendency to remain unchanged and is therefore said to possess certain inertia. As a result, the resistance value takes a small amount of time to change its value and does not respond immediately to variations in the excitation waveform. We have obtained the switching times of the linear Ion drift model and VTEAM model for various windows as shown in Table 4.0. It is seen that the VTEAM model has a smaller switching time in the order of *n*s as compared to the linear ion drift model which has switching time in the order of microseconds. Table 3.0 shows the parameters used in the analysis of the memristor model.

PARAMETER	VALUE
Model	0-Linear ion drift 4-VTEAM
Window type	0-No window 1-Jogelkar 2-Biolek 3-Prodromakis 4-Katvinsky
dt	7.00E-09
Init_state	0
R_{off}	1000
R_{on}	100
D	3.00E-09
w_multiplied	1
P_coeff	2
J	1.5
p_window_noise	1.00E-18
x_c	1.07E-09
a_on	2.00E-09
a_off	1.20E-09
K_on	-0.000085
K_off	5.00E-04
Alpha_on	3
Alpha_off	1
V_on	-0.2
V_off	0.02
X_off	3.00E-09

Table3.0. shows the parameters used in the analysis of the memristor models

WINDOW TYPE	LINEAR ION DRIFT (0-1) *μs*	VTEAM (0-1) *ns*	LINEAR ION DRIFT (1-0) *μs*	VTEAM (1-0) *ns*
NO WINDOW	45.97	33.45	44.77	33.25
JOGELKAR	0.126 (spike)	152	0.123 (spike)	24.91
BIOLEK	139.42	218	343.44	265.17
PRODROMAKIS	252.5	(spikes)	248.5	(spikes)
KATVINSKY	273	(weak 0)	264.93	(weak 0)

Table4.0. shows the switching time of Linear ion model and vteam model for various windows.

B. Power

The average power of the linear ion drift model and VTEAM model were calculated for different windows as shown in Table 5.0. The power of the different voltage levels used for the MLC was also calculated for the VTEAM model as shown in table 6.0 and the linear ion drift model as shown in table7.0. The instantaneous power dissipated by the memristor is given by

$$\text{Average Power} = \int (p(t))/t \quad (9)$$

$$p(t)=M(q(t))i^2(t) \text{ or } p(t)= W(\varphi(t))v^2(t) \quad (8)$$

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WINDOW TYPE	LINEAR ION DRIFT POWER AVG (nW)	VTEAM POWER AVG (μW)
NO WINDOW (-1.8V, +1.8V)	129.5	100
JOGELKAR (-5V, +5V)	999.6	2045
BIOLEK (-2.1, +2.1V)	176.3	145.6

Table5.0 shows the average power of linear Ion drift model and VTEAM model for No window, jogelkar window and Biolek window

VOLTAGE(V)	POWER (mW)
0.2	**2.923**
1	**1.660**
1.33	**1.288**
1.6	**1.33**

Table6.0. shows the power of different voltage levels used for the MLC in table 1.1.(R_{on}=100, R_{off}=1000, VTEAM model window-0)

VOLTAGE(V)	POWER (μW)
0.2	**6.850**
1	**8.086**
1.33	**9.422**
1.6	**11.13**

Table7.0. shows the power of different voltage levels used for the MLC in table 1.0.(Ron=100, Roff=5000, Linear ion Drift model window-0)

VI. CONCLUSION

This research work presents a novel design of memristor-based multi-level memory cell and its Cross-bar architecture. The developed memory cell demonstrates low power dissipation and high-speed operation. Necessary interface circuits such as write driver and read circuit have been designed to perform the multi-level write and read operations. The operation of the memory cell has been investigated using the HP memristor model namely linear ion drift model as well as simple, theoretically efficient, generic memristor model called voltage threshold adaptive memristor model (VTEAM). The results demonstrate that VTEAM model based memristor cell requires less power to perform write/read operation as well as operates at higher speed than linear ion drift model for the considered voltage levels used for storage of data. Though the multi-level cell has been designed using bipolar memristor, with minimal changes, the design can be adapted to a unipolar memristive device.

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