A 1000 Mhz Low Power And High Speed 8-Bit Flash ADC Architecture using 90nm Cmos Technology

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Abstract-. The design objective is to implement a Low power, High speed and High resolution Flash ADC with increased sampling rate. To make this possible the blocks of ADC are analyzed. The resistive ladder, comparator block, encoder block are the major modules of flash ADC. Firstly, the comparator block is designed so that it consumes low power. A NMOS latch based, PMOS LATCH based and a Strong ARM Latch based comparators were designed separately. A comparative analysis is made with the comparator designs. Comparators in the design is reduced to half by using time domain interpolation. Then a reference subtraction block is designed to generate the subtraction value of voltages easily and its given as input to comparator. Then a more efficient and low power consuming fat tree encoder is designed. Once all the blocks were ready, a 8 bit Flash Analog to Digital Converter was designed using 90nm CMOS technology and all the parameters such as sampling rate, power consumption, resolution were obtained and compared with other works.

I. INTRODUCTION

Fields of ADC usage include medical, radar, data acquisition.

Modules of general flash ADC

- Reference r-ladder
- Voltage input
- Comparator
- Encoder logic

To make the Flash ADC more efficient, we have dealt with some basic key issues of Flash ADC such as speed, performance, area and power consumption by using some techniques.

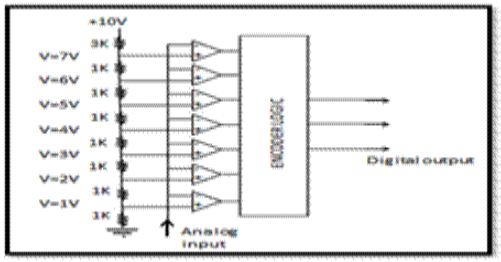

Fig. 1. Flash ADC Block

II. PROPOSED SYSTEM

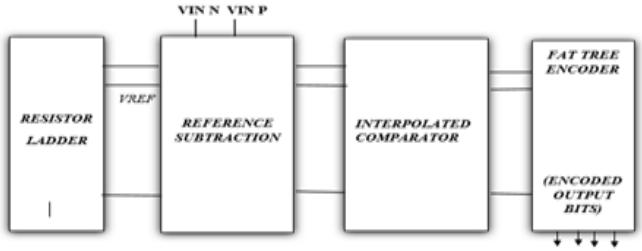

Fig 2. Block Diagram for the Flash ADC

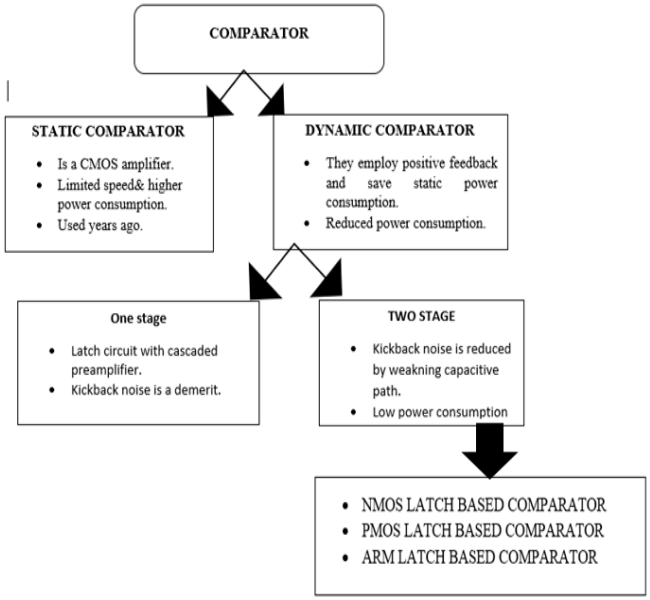

Fig 3. Flow for the Comparitive Analysis of the Comparator

Design Of Two Stage Dyamnic Comparator With Nmos Latch

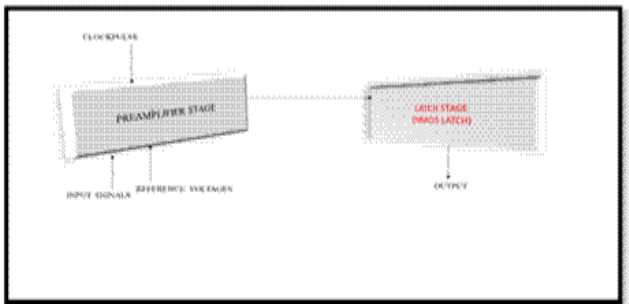

Fig 4. Twostage Dynamic Comparator with NMOS Latch

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To set the gain higher, the transistor M3,4 are chosen to have a appropriate size. But the delay parameters are controlled by offset which can be overcome by a pmos latch.

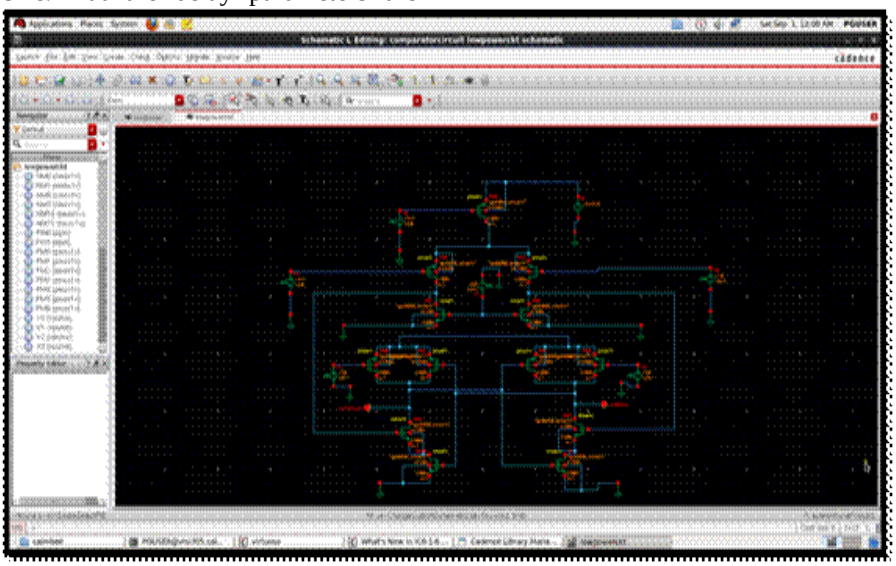

Fig 5. Schematic Of NMOS Latch Based Comparator In Cadence

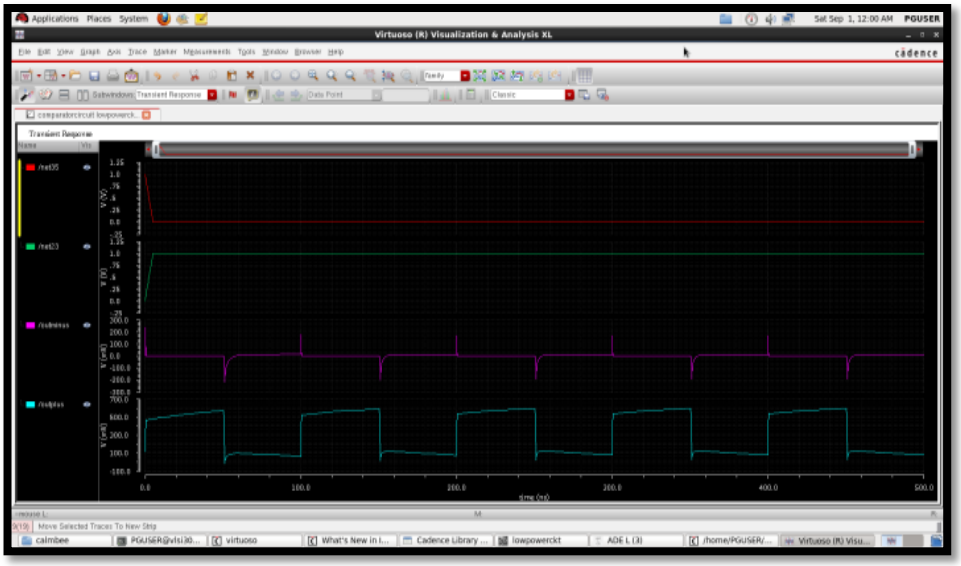

Fig 6. Output Obtained For Precharge And Evaluation

Fig 7. Power Consumption Of Nmos Latch Based Comparator

Design Of Two Stage Dyamnic Comparator With Pmos Latch

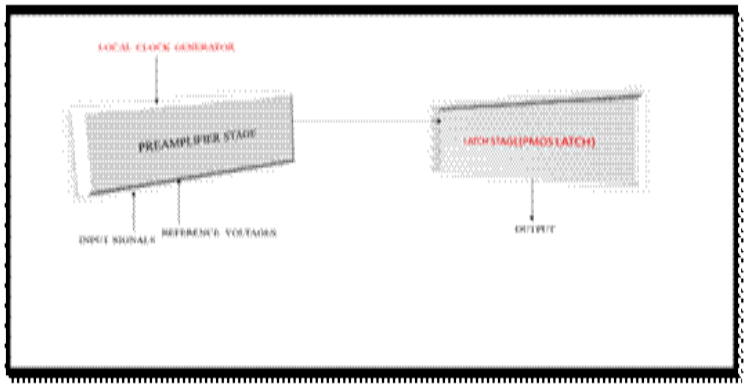

Fig 8. Twostage dynamic comparator with pmos latch and local clock generator.

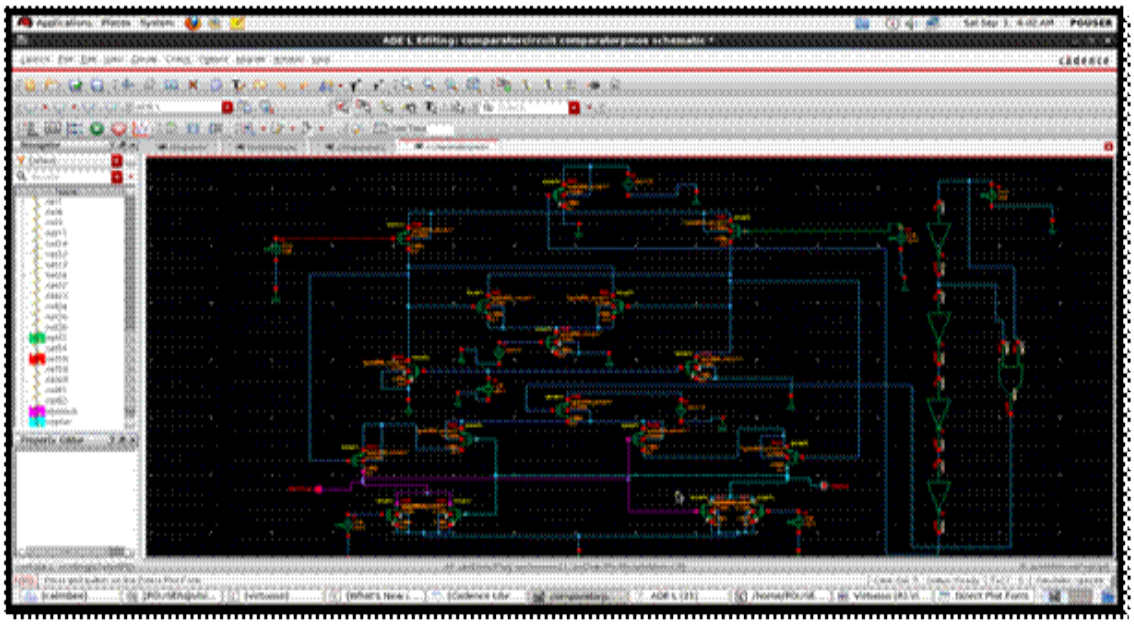

Fig 9. Dynamic Comparator With Pmos Latch And Local Clock Generator

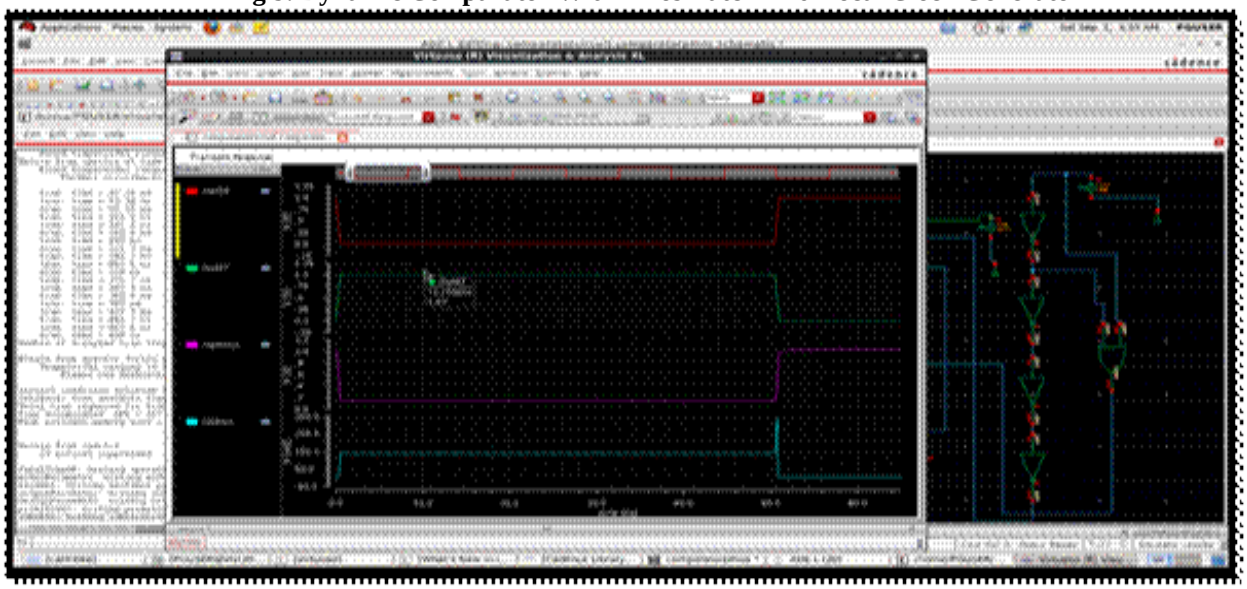

Fig 10. Output Obtained For Pmos Latch Based Comparator

A optimum delay is being defined in this type of comparator.It consists of a preamplifier stage where a local generator is designed which plays a major role.In the evaluation phase a predetermined delay is defined.

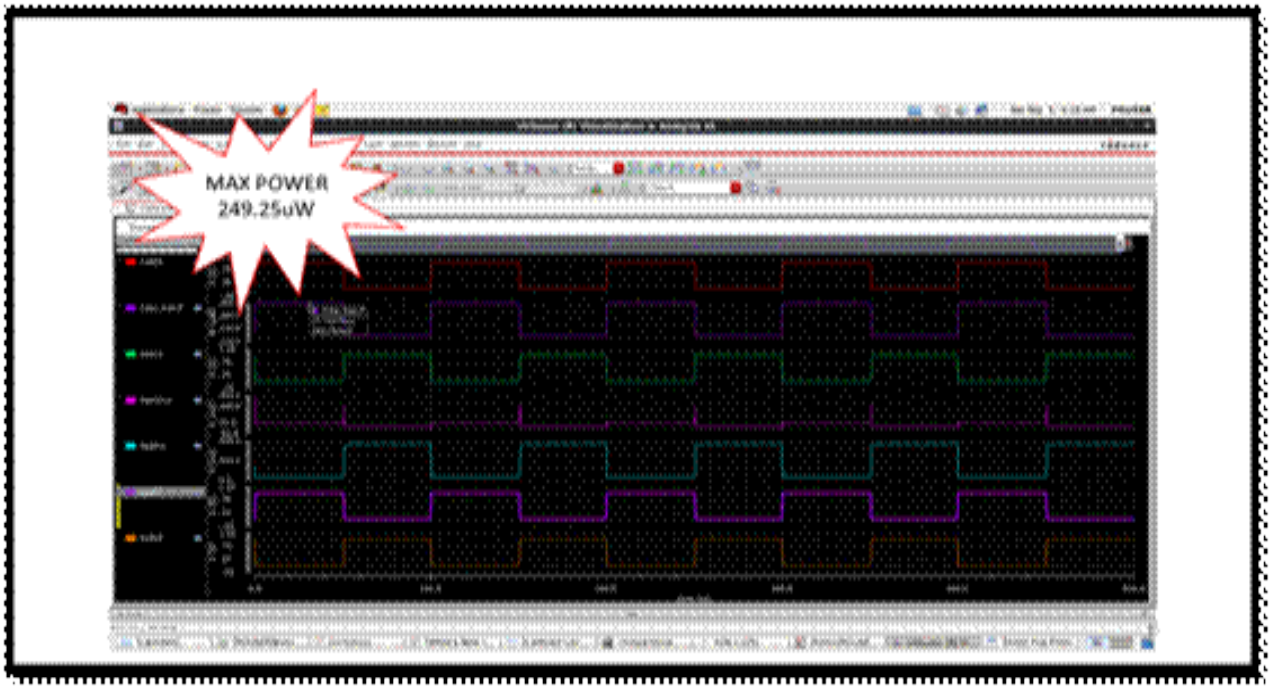

Fig 11. Power Consumption Of Design Based On Pmos Latch

Design Of Two Stage Dyamnic Comparator With Strong Arm Latch

The strong ARM latch is does consumes zero static power,rail to rail output is directly produced,the input referred offset arises from one differential pair.This makes the Strong ARM latch popular.

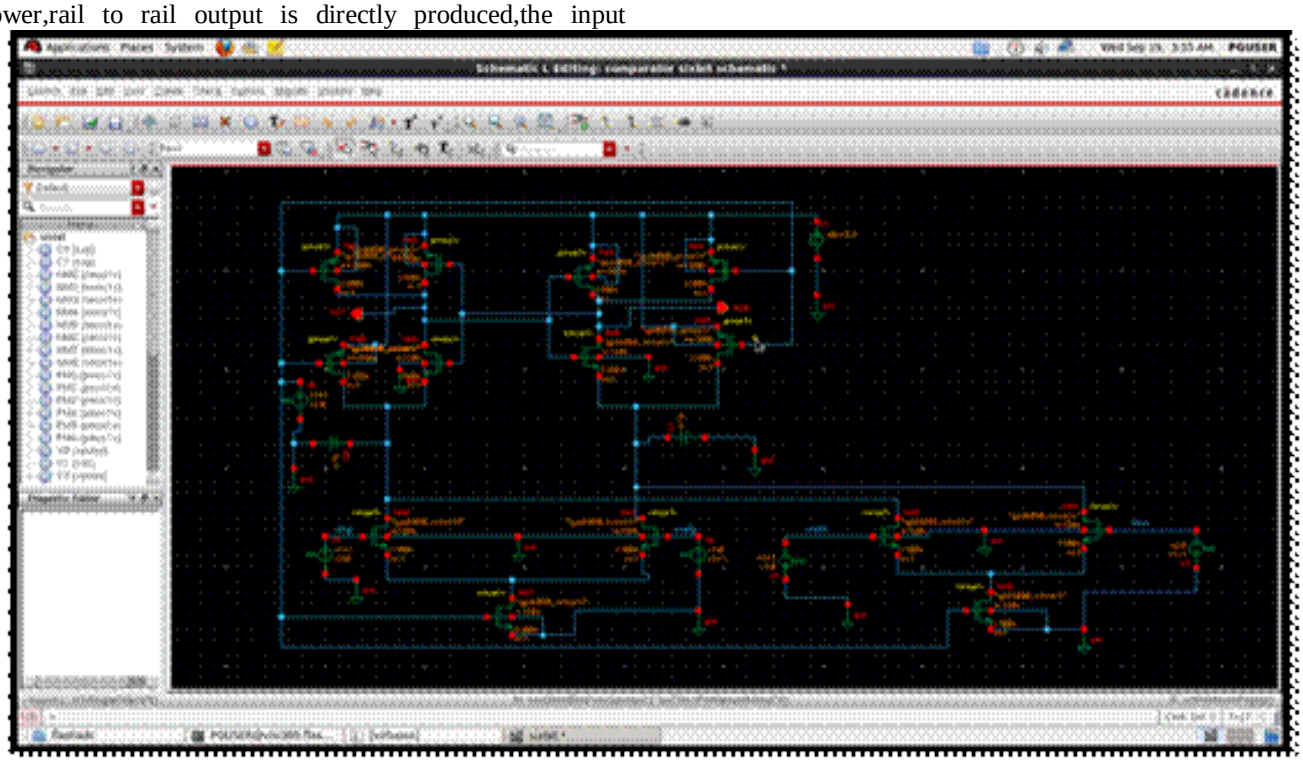

Fig 12. Comparator Based On Strong Arm Latch

In the reset phase,clock is low and the nodes A,B,C,D is precharged to vdd where transistor M2 is off.In the next phase-amplification mode,clock goes high,transistor M1 and M2 are on.This phase provides voltage gain.

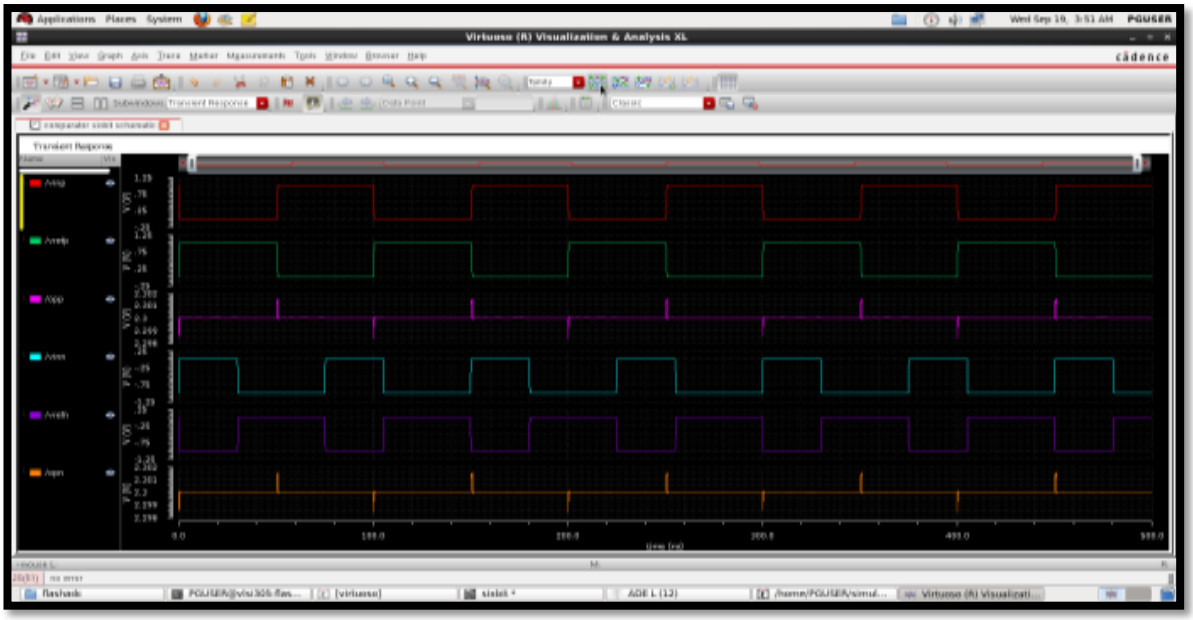

Fig 13. Output Obtained For Strong Armlatch Based Comparator

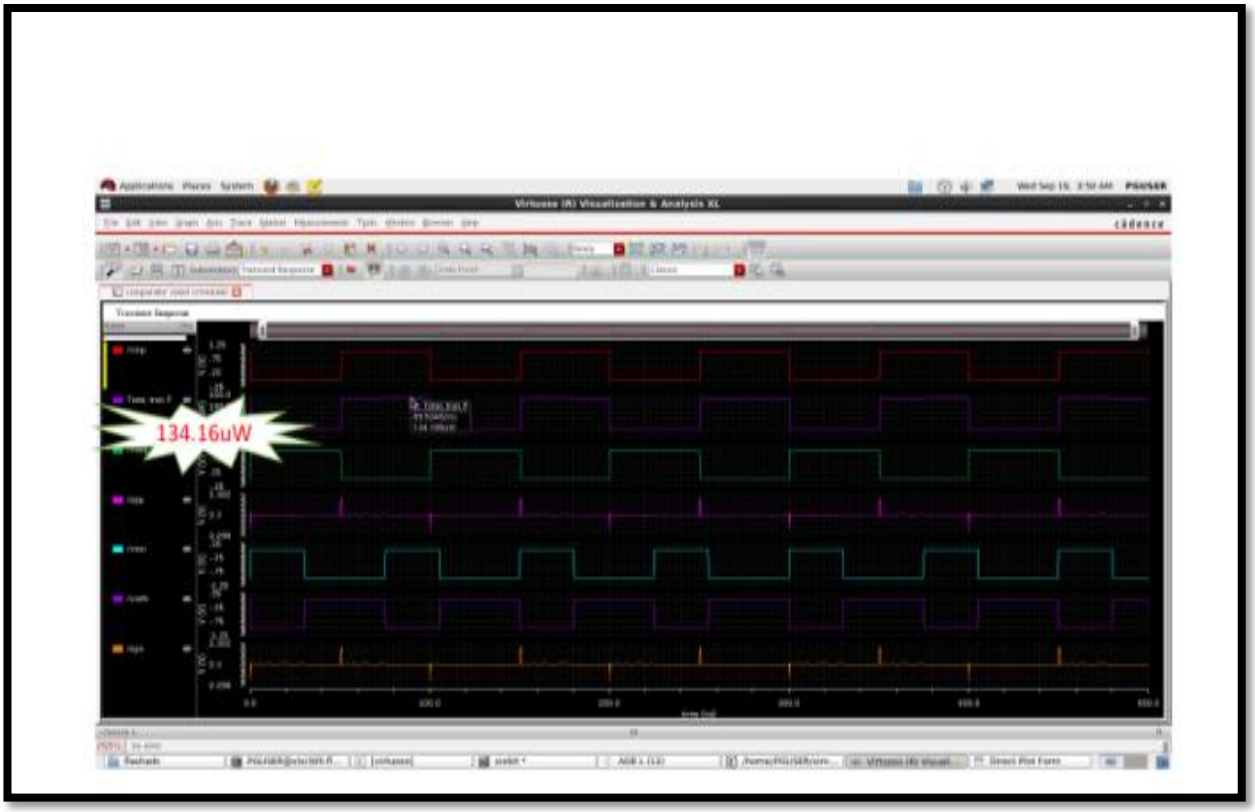

Fig 14. Power Consumption Of The Design

Comparitive Analysis Of Powerconsumption Among The Comparators

Since ARMLATCH BASED comparator is consuming the least performance and has improved speed,We prefer this comparator for our proposed ADC design.

TABLE 1.

S.NO	COMPARATOR TYPE	POWERCONSUMPTION
1.	NMOS LATCH BASED	838.63 µW
2.	PMOS LATCH BASED	249.25 Mw
3.	ARM LATCH BASED	134.16 µW

Thus , We prefer the Strong ARM Latch comparator(Lowest power consuming) in the proposed Flash ADC design

III. TIME DOMAIN INTERPOLATION OF THE COMPARATOR :

Its performing interpolation on a sequence of time domain samples.The time-domain interpolation follows the fact that, Vin +ve, here required for the flash adc is normally (2^N)-1. But after time domain domain interpolation it has been halved as 1/2(2^N)-1.

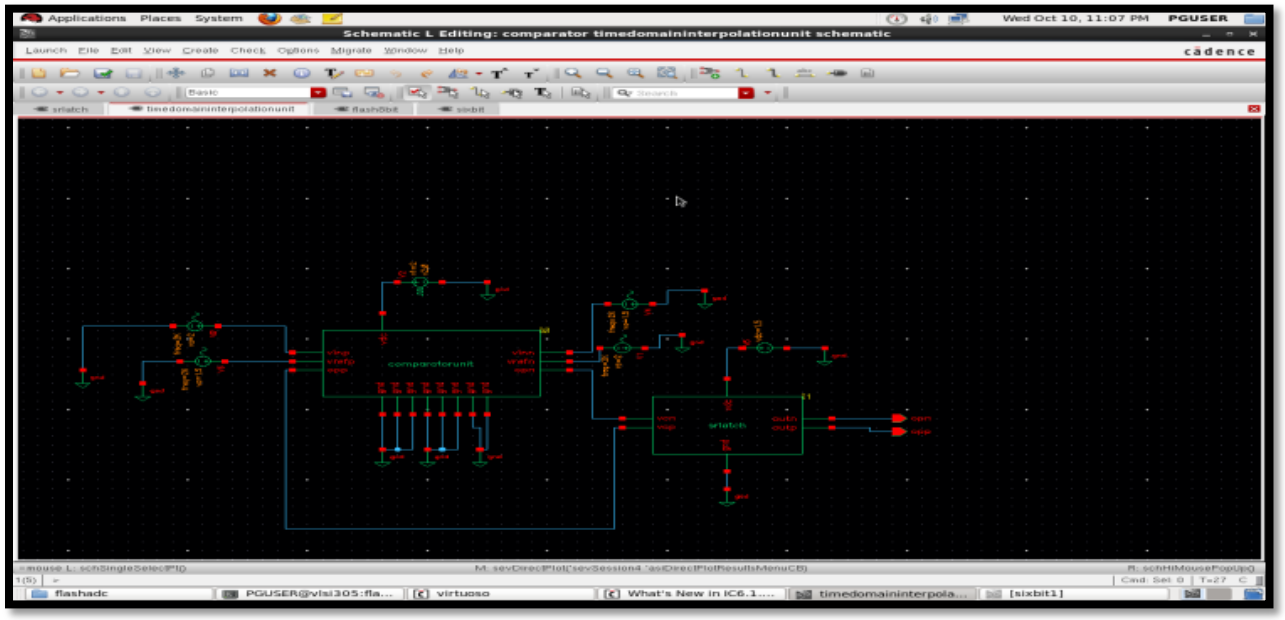

Fig 15. Time Domain Interpolation Unit In Cadence

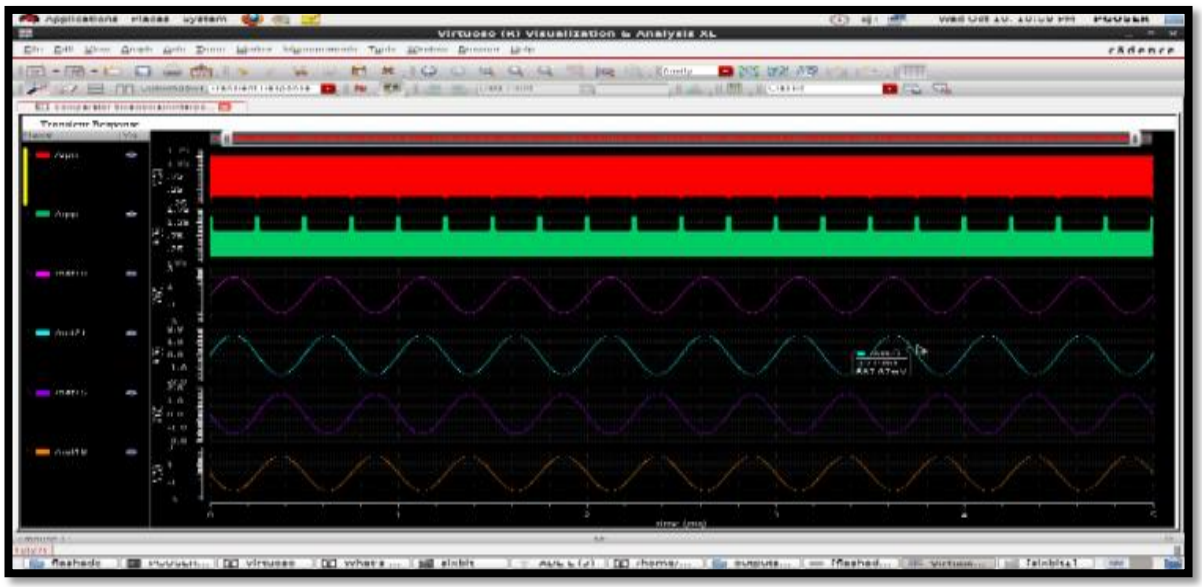

Fig 16. Output Obtained For The Time Domain Interpolation

IV. FAT TREE ENCODER & RESULTS

Its preferred that is highly suitable for the ultrahigh speed flash ADCs and the speed is improved by a factor of 2.

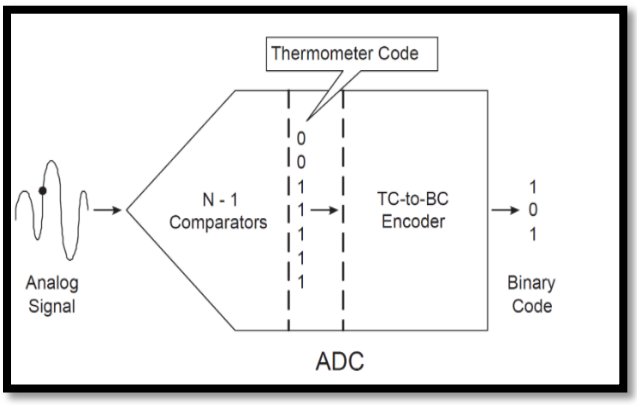

Fig 17. Fat Tree Encoder Block

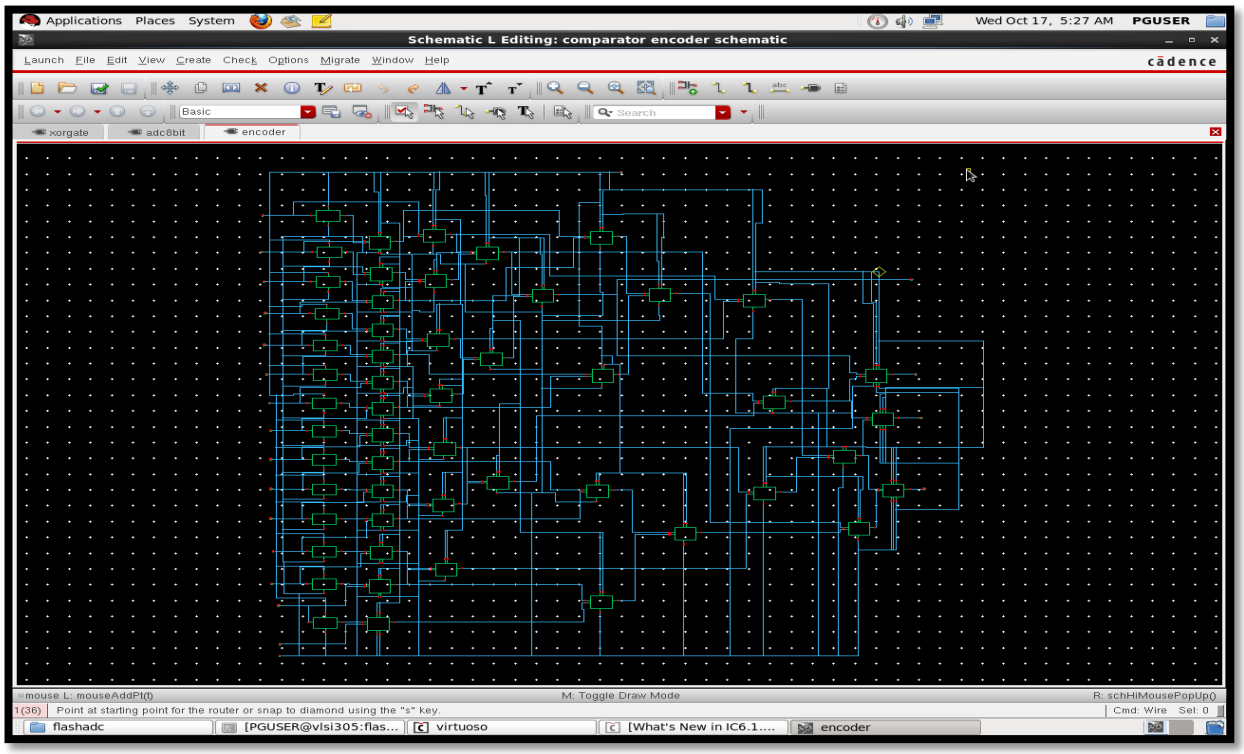

Fig 18. Implementation Of Encoder In Cadence

V. PROPOSED 8BIT FLASH ADC

The Reference generated is subtracted with the voltage input and is fed to the comparator.The output generated from the comparator, which is of digital bits and its encoded by using fat tree encoder.This fat tree encoder has higher performs, speed and the area it consumes is lower. Thus the Flash ADC is analyzed by the transient response in cadence and the power consumed, sampling rate, resolution and SNR are being calculated.

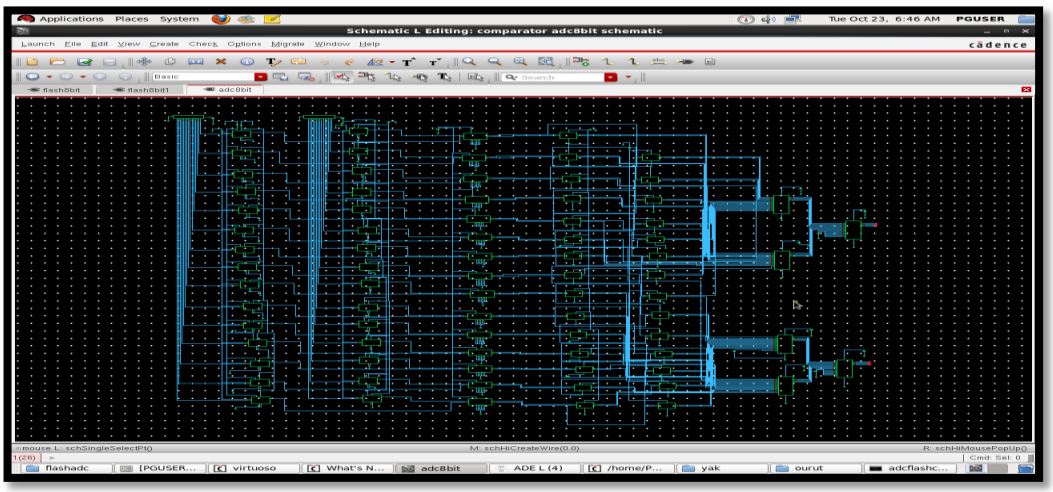

Fig 19. 8BIT Flash ADC

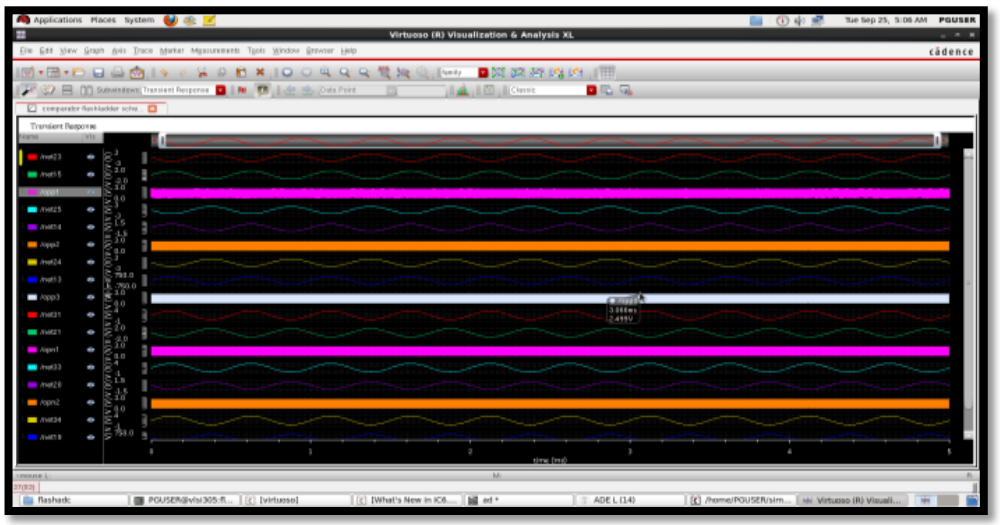

Fig 20. Analog Input Fed

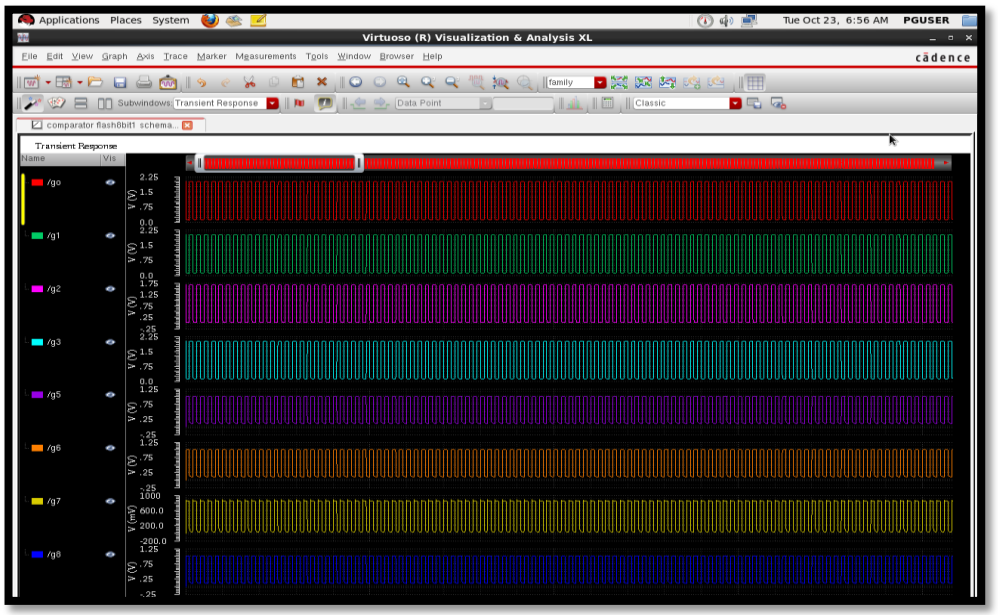

Fig 21. Converted Output Of The ADC

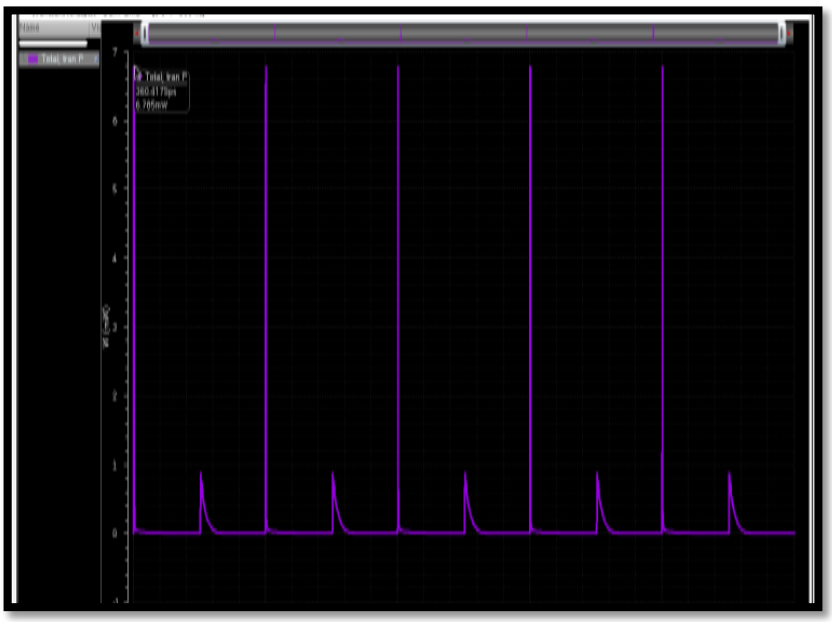

Fig 22. Power Plot For The Designed ADC

VI. CONCLUSION

TABLE 2.

PARAMETERS ANALYZED	PROPOSED DESIGN
Resolution	8
Power consumption	6.785mW
Sampling rate	1000MHZ
SNR	49.924dB
Architecture	Time domain interpolated ADC
Technology	90 nm

VII. COMPARITIVE ANALYSIS

Parameter analysed	Proposed design	[3]	[4]	[5]
Resolution	8	6	10	5
Power consumption	6.785mW	98mW	68.3mW	6.7mW
Sampling rate	1000MHZ	3.5GS/s	100MHZ	0.6 GS/s
SNR	49.924dB	31.18dB	56.4dB	--
Technology	90nm	90nm	90nm	90nm

VIII. CONCLUSION

This research paper analyzes the Flash ADC the parameters transient response, power consumed, sampling rate, resolution and SNR using Cadence EDA. And also we compare the different parameters analysed using 90nm technology. By comparing with existing methods, this circuit provides higher SNR. In future we analyse by using different technology (i.e 45nm, 65nm).

IX. REFERENCES

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