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FPGA Implementation of Adaptive Multiplier-Based Linear Image Interpolation

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Abstract: ***This work provides an image interpolation for multimedia applications by utilizing an adaptive multiplier-based stepwise linear interpolation with clam filter. Image interpolation is also termed as image up-scaling. Generally, while enlarging an image some vacant bit positions are introduced and due to this empty pixel positions, the quality of the image is decreased. Therefore to maintain the quality of the image, new pixels are introduced and those pixels are used to fill the vacant bit positions by using interpolation techniques. In the adaptive interpolation techniques, edge pixels are identified and filtered at prior to the interpolation process. This will improve the quality of the interpolated image. However, the adaptive interpolation scheme increases the complexity of the system. To reduce the complexity, this work uses low complexity stepwise linear interpolation and to maintain the quality it uses multiplier-based linear stepwise (MBLSI) and edge enhancement technique. The experimental results demonstrate that the complexity of the proposed work is less as compared with other related work as well as the quality is also maintained. The proposed work utilizes 275 LUTs to provide the average peak signal to noise ratio (PSNR) of 20.44 dB and structural similarity index (SSIM) as 0.8250. This proposed work increases the PSNR by 0.89 dB from the conventional multiplier-based stepwise linear interpolation. Further the proposed interpolation algorithm utilizes less number of resources in field programmable gate array (FPGA) by comparing with other related interpolation techniques.***

Index Terms: ***Up-scaling, Resolution, PSNR, LUT, Edge-detection***

I. INTRODUCTION

The goal of image interpolation is to maintain the resolution of the given image and it is also used to increase the resolution in the high resolution (HR) grid by introducing new pixels using old pixels neighbour [1]. In multimedia, image interpolation is basic task to improve the quality of both still and video images and it is widely used in digital photography [2]. Ii is also used in medical image processing, remote sensing and other consumer electronics like mobile phone [3]. Image interpolation is also used in different kinds of image processing operations like image warping, image enhancement and image registration [4].

Image interpolation is classified into two main categories such as non-adaptive and adaptive image interpolation techniques [5]. The non-adaptive image interpolation employs constant and fixed algorithm throughout the entire interpolation process. But the adaptive interpolation treats pixels differently based on the quality of the pixels. Therefore the adaptive interpolation techniques remove blurring and other edge artifacts while interpolating image. That is, the adaptive technique is mostly used in the process of improving image resolution. However, the adaptive interpolation technique is complex as compared with the non-adaptive image interpolation technique. Many researchers have developed different types of adaptive interpolation techniques to improve the quality as well as to reduce the complexity in the past two decades. In most of the image processing applications, the interpolation operation is embedded in consumer products like still camera in the form of integrated circuits (ICs) [6]. For fabricating any ICs the designers use complex metal oxide semiconductor very large scale integration (CMOS VLSI) technology as it performs fast and consumes low power. The VLSI design consists of two phases as front-end design using FPGA and back-end design using application specific integrated circuit (ASIC). As FPGA is fast on producing end-user equipment and it is reconfigurable [7], it is mostly utilized in real-time image processing applications. Furthermore, as one of the design goals of VLSI design is less area and nowadays many of the consumer products are tiny in size most of the developers prefers less size ICs. This proposed work aims to reduce the number of look-up tables (LUTs) on FPGA by using low complexity linear interpolation. All conventional interpolation schemes like nearest neighbour, linear, bilinear and bi-cubic interpolation techniques are non-adaptive interpolation methods. Among these interpolation schemes bi-cubic is efficient but it is complex and therefore it is not preferred for low-complexity FPGA implementation [8]. The nearest neighbour algorithm is simple but not good in interpolation quality. Thus, for reducing complexity and area-efficient FPGA implementation linear interpolation method is preferred. Conventional stepwise linear interpolation is a non-adaptive technique and is efficient in complexity but it introduces blurry images while interpolating the image. The proposed work suggests a novel system for improving the quality of the interpolated image by filtering edge-pixels at prior the interpolation process and called as adaptive stepwise linear interpolation. Further the proposed interpolation scheme is realized in virtex 2 FPGA. The remaining portion of this paper is organized as follows. Section 2 covers a detailed survey on related works on linear interpolation, section 3 provides the details of proposed edge-based stepwise linear interpolation, section 4 deals with the experimental results of the proposed adaptive stepwise linear interpolation and other related linear interpolation techniques and section 5 presents conclusion and future scope of the edge-based stepwise linear interpolation technique.

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II. RELATED WORKS

This chapter briefs the achievements of recent related adaptive (edge-based) interpolation techniques based on their quality and complexity. Adaptive interpolation methods differs the algorithm based on the internal structure of the pixels to be interpolated.

Linear interpolation for CMOS sensor is proposed by [9]. This method is used to improve the resolution on sensor's image. This requires less number of components. Linear interpolation is also used for image reconstruction by reconstructing transform coefficients [10]. The transform coefficient-based interpolation technique provides higher accuracy on image reconstruction. Linear image interpolation for enhancing medical images is presented by [11] using auto correlation function to estimate the unknown pixels. This method is computationally efficient than B-spline interpolation scheme. Other linear interpolation algorithms are proposed [12] and [13] by utilizing space invariant scheme and optimal shift scheme respectively to perform image up-scaling. The complexity of linear interpolation is less as compared with non-linear interpolation techniques.

In the conventional linear convolution interpolation, the complexity of the algorithm depends on the order of linear convolution equations. Several higher order linear convolution interpolation algorithms are proposed in the past two decades to achieve high quality on interpolated image. A polynomial convolution interpolation [14] is by using third order equation. This method achieves higher PSNR than other related interpolation algorithms, but the complexity is high. Further this algorithm utilizes many number of neighbouring pixels that is, 16 to introduce a new pixel. The extension of this work [15] utilizes the same third order approximation and it reduces the complexity from the previous third order equation [14]. Iterative linear interpolation [16] provides low complexity as compared with previous methods [14], but the quality is lower than the previous methods [14] and [15]. Linear interpolation is also used for word processing applications [17] using bilinear algorithm.

An extension of linear interpolation is the bilinear interpolation scheme. A bilinear image interpolation is proposed by [18] to object recognition by smooth out the image. Bandlet transform-based bilinear interpolation [19] is used for image zooming. This method provides better result than wavelet transform-based interpolation scheme. Another bilinear interpolation scheme is utilized by [20] to improve the resolution on of the output image of the graphic processor. This method utilizes Wallis transform to improve the speed of operation. A piecewise linear interpolation based on pattern weight [21] to improve the quality of image. This provides higher quality as compared with bi-cubic interpolation proposed by [22].

An edge-based linear image interpolation is developed by [23] and it utilizes maximal Eigen. This method is used to reduce edge blurring problem in the interpolated image. Image up-scaling using edge-based bilinear is provided by [24]. This method filters the edge pixels at prior the up-scaling process by using sharpening filter to provide higher accuracy on the reconstructed image. The edge pixels are identified by gradient operators. An edge-based bilinear interpolation [8] is implemented by using sharpening filter. This method is realized by using TSMC CMOS 0.13 µm technology and it utilizes 6.67 k gates. Another edge-based bilinear interpolation using both sharpening and clamp filter is realized by [25] and it utilizes 6.08 gates on CMOS 1.3 µm technology, but the quality of this interpolation scheme is less than the previous bilinear interpolation [8]. Adder-based stepwise linear interpolation [26] is designed and realized by using CMOS 0.18µm technology and it requires 552.18 µm on ASIC to achieve maximum PSNR of 32.15 dB.

FPGA implementation of bilinear interpolation is proposed by [27] for zooming digital images. This implementation requires 329 configuration logic blocks (CLBs) on FPGA. Another FPGA implementation for image interpolation is developed by [28] using piecewise linear interpolation. It utilizes 310 look-up tables (LUTs) on FPGA. An edge-based bilinear interpolation using low complexity I model kernel for clamp filter is implemented by [29]. Sharpening filter-based edge bilinear interpolation using this low complexity kernel utilizes less amount of LUTs on Kintex FPGA as compared with the previous edge-based bilinear proposed by [25]. Further, adaptive adder-based stepwise linear interpolation [30] is suggested to improve the PSNR from the conventional adder-based stepwise linear interpolation [26] by using 3x 3 clamp filter.

III. ADAPTIVE MULTIPLIER-BADSED LINEAR INTERPOLATION

Linear interpolation algorithm uses first-order equations and it utilizes only two known pixels to introduce a new pixel. Therefore linear interpolation is simple algorithm and it requires simple circuits and low complexity. However, the conventional linear interpolation is not very good on interpolated image so some alternative methods are utilizes in the recent years. This work utilizes clamp filter (3 x 3 kernel), sigmoidal edge detector and multiplier-based stepwise linear interpolation [26] to improve the PSNR from the conventional linear interpolation and to reduce the complexity of interpolation from the recently developed edge-based bilinear [8] and Lagrange interpolation [31] algorithms.

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Figure 1 illustrates conceptual block diagram of proposed adaptive multiplier-based stepwise linear interpolation.

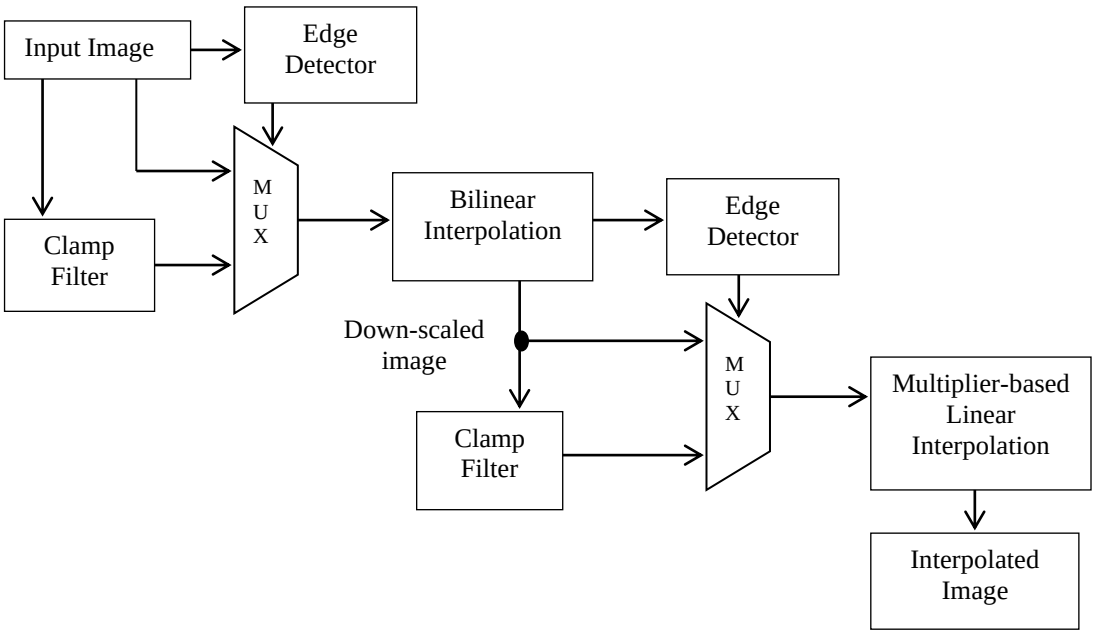


Figure 1: Conceptual diagram of Adaptive Multiplier-based Linear Interpolation algorithm for image processing

As shown in Figure 1 the proposed multiplier-based interpolation is performed by using sigmoidal edge detector [8], 3 x 3 clamp filter, bilinear interpolation [25] and multiplier-based stepwise linear interpolation [26]. The sigmoidal edge-detector identifies the quality of the edge pixels to be interpolated. Based on the quality of the edge pixels, the multiplexer allows either direct pixel from the input image or filtered image for further image interpolation. Bilinear interpolation is used to perform down scaling and the down scaling image. Further, Multiplier-based interpolation is used to perform up-scaling. Equation (1) represents the bilinear interpolation

$$Y'_{(k,1)} = (1-cx)\times(1-cy)\times Y_{(m,n)} + (1-cx)\times cy\times Y_{(m,n+1)} + cx\times(1-cy)\times Y_{(m+1,n)} + cx\times cy\times Y_{(m+1,n+1)} \quad (1)$$

Where, cx and cy is the distance between horizontal and vertical distance from the old pixel to the interpolation point respectively. $Y_{(m,n)}$is the filtered image.

Multiplier-based stepwise linear interpolation is performed by Equation (2)

$$Y''_k(m,n) = p_1 + (p_2 - p_1) * (k_1/k) \quad (2)$$

Where $k = k_1 + k_2$ (3)

k_1 is the distance between old pixel (p_1) and new pixel (Y''_k) and
k_2 is the distance between old pixel (p_2) and new pixel (Y''_k)
Y''_k is the up-scaled image, p_1 and p_2 are old pixels from the down-scaled image.

Equation (4) represents the kernel of 3 x 3 clamp filter

$$Clamp\ (3*3) = \begin{bmatrix} 1 & 1 & 1 \\ 1 & CC & 1 \\ 1 & 1 & 1 \end{bmatrix} \quad (4)$$

Where CC is clamp coefficient which can be set by user based on the characteristic of the image [25]. The filtered image$Y(m,n)$ is derived from the original image y (m,n) as shown in Equation (5).

$$Y(m,n) = \frac{y(m,n)*\begin{bmatrix} 1 & 1 & 1 \\ 1 & CC & 1 \\ 1 & 1 & 1 \end{bmatrix}}{CC+8} \quad (5)$$

The proposed adaptive multiplier-based stepwise linear interpolation is simulated by MATLAB and MATLAB Simulink. Xilinx System Generator and Xilinx ISE are used to implement the design on Virtex-2 FPGA

IV EXPERIMENTAL RESULTS AND COMPARATIVE ANALYSIS

The proposed method of image interpolation and other related interpolation algorithms are evaluated based on their PSNR and SSIM values [32]. Further the complexity of the algorithms is measured by using number of LUTs utilized by different algorithms on FPGA. To analyse the characteristics of image interpolation algorithms, 24 Kodak colour images (768×512) are used (www.r0k.us/graphics/kodak) as shown in Figure 2.

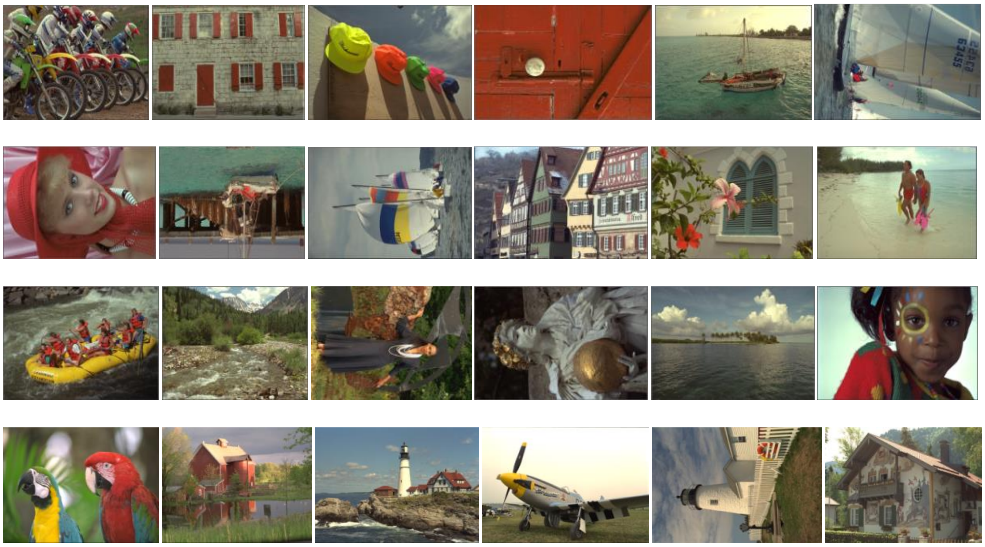
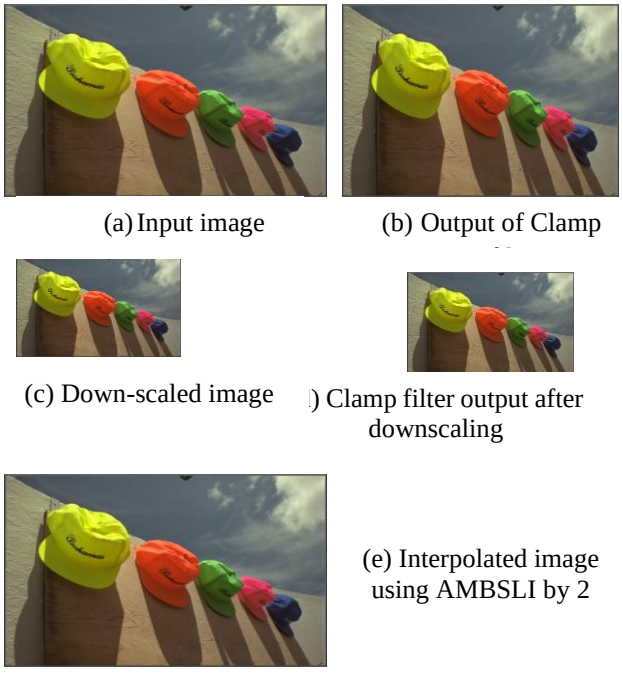


Figure 2: Input images considered for experimentation

Figure 3 illustrates the sample output of proposed AMBSLI on "cap" image. Figure 3(a) is the original input image, Figure 3 (b) is the output of 3 * 3 clamp filter, Figure 3 (c) is the down-scaled image using bilinear algorithm for the interpolation factor of 0.5. The downscaled image is again filtered by using the clamp filter as shown in Figure 3 (c). Further, the filtered image is up-scaled by the proposed AMBSLI for the scaling factor of 2 as shown in Figure 3 (e). Table I describes the PSNR and SSIM values of the proposed image interpolation and related algorithms.

Table I: Comparison of average PSNR (dB) and SSIM value for the various interpolation methods using 24 Kodak images

Interpolation Algorithm	PSNR	SSIM
ABSI (Huang and Chang,2016) [26]	19.44	0.7955
AABSI algorithm (Moses 2018) [30]	20.12	0.8207
MBSI algorithm (Huang and Chang,2016) [26]	19.55	0.8014
Filter-based MBLI (proposed)	19.85	0.8113
Edge-based MBLI (proposed)	**20.44**	**0.8250**



(a) Input image (b) Output of Clamp

(c) Down-scaled image) Clamp filter output after downscaling

(e) Interpolated image using AMBSLI by 2

Figure 3: Sample output image of proposed AMBSLI

From Table 1, it is understood that the proposed multiplier-based linear interpolation techniques provide higher accuracy in term of PSNR and SSIM by comparing with other related techniques such as adder-based [26] adaptive-adder based [30] and multiplier-based interpolation [26].

Table 2 and Table 3 illustrate the comparison between the proposed filter-based MBSLI (FMBSLI) and adaptive MBSLI interpolation respectively and other related interpolation techniques such as clamp filter(CF)-based (T-model) bilinear (TFBBL) [25], CF-based first-order polynomial convolution interpolation (FBFOPCI) [33], CF-based Lagrange (FBLG) [31] , CF (3 * 3 model) - based bilinear (FBBL) [34] , CF-based adder-based stepwise linear interpolation (FBABSI)[35], CF (2 * 3 model) [31] - based bi-cubic (FBBC), clamp filter (T-model) – based Lagrange (TFBLG) [31] , T-model sharp filter-based edge-based bilinear (TSFEBBL) [8] , I model sharp filter and edge-based bilinear (ISFEBBL) [29], I-model combined filter and edge-based bilinear (ICMFEBBL) [29] and the proposed adaptive multiplier-based stepwise linear interpolation (AMBSLI) based on different area utilization parameters on FPGA parameters.

Table 2: FPGA parameters on Filter-based interpolation techniques

Interpolation method	Filter type	FPGA	No. of LUTs	Slice Registers	Slices	Memory usage (MB)
TFBBL [25]	CF T	Virtex - 2	266	268	92	1017
FBFOPCI [33]	CF 3 * 3	Virtex - 6	260	NA	87	NA
FBLG [31]	CF 2 * 3	Virtex - 2	258	196	103	1026
FBBL [34]	CF 3 * 3	Virtex - 2	247	263	121	1022
FBABSI [35]	CF 3 * 3	NA	242	191	102	NA
FBBC [31]	CF 2 * 3	Virtex - 2	239	268	109	1022
TFBLG [32]	CF T	Virtex - 2	238	200	105	1026

Table 3: FPGA parameters on Adaptive edge-based interpolation algorithms

Interpolation method	Parameters						
	FPGA	No. of LUTs	FFs	Slice Registers	Slices	LUT FF pair	Memory Usage (MB)
TSFEBBL [8]	Kirtex - 7	341	82	92	116	382	838
ISFEBBL [29]	Kirtex - 7	298	82	89	100	330	837
ICMFEBBL [29]	Kirtex - 7	580	82	92	179	629	841
AMBSLI [Proposed]	Virtex - 2	275	79	90	98	356	812

Based on Table 2, the proposed clam filter (3 * 3 kernel)-based multiplier-based stepwise linear interpolation utilizes less number of resources particularly less number of LUTs on FPGA. The proposed filter-based MBSLI reduces 37 LUTs from the filter-based bilinear interpolation [25]. This shows that by using the proposed interpolation is a choice for developing area-efficient filter based-interpolator. Based on Table 3, the proposed adaptive edge-based multiplier-based stepwise linear interpolation uses less number of LUTs as compared with other edge-based bilinear interpolation techniques. So the linear interpolation is a best one for implementing area-efficient design for interpolation. The proposed adaptive MBSI reduces 66 LUTs from the sharpening filter and edge-based bilinear interpolation [8].

V CONCLUSION

This work demonstrates the implementation of an area-efficient image interpolation and its realization in FPGA. The proposed edge-based stepwise linear interpolation outperforms other related interpolation algorithms like conventional adder-based stepwise linear interpolation, conventional multiplier-based stepwise linear interpolation, edge-based adder adder-based stepwise linear interpolation in terms of PSNR and SSIM. For instance the proposed interpolation algorithm increases SSIM by 0.0236 from the conventional multiplier-based stepwise linear interpolation. Further, the FPGA implementation of this proposed algorithms such as clam filter-based multiplier-based stepwise linear interpolation and adaptive multiplier-based stepwise linear interpolation decrease number of resources in FPGA by comparing with other related filter-based and edge-based algorithms. Therefore this proposed adaptive multiplier-based stepwise linear interpolation is suitable for high performance linear interpolation as well as low complexity interpolation application. Furthermore, there is a scope on reducing complexity of the proposed architecture by utilizing simple kernel for clamp filter and improving the quality of the adaptive interpolation by filtering and interpolating the edge-pixels based on their orientation or direction. So the reconfigurable adaptive-edge-based interpolation is suitable for low complexity multimedia applications like still camera and camcorder.

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