Implementation of Low Power and High Performance Adder Circuits

B. Jaya Lakshmi, R. Ramana Reddy

Abstract: ***Adders plays a crucial role for implementing the arithmetic operations in analog and digital circuits. These adders are widely used in arithmetic systems, DSP systems, etc. The proposed dual mode square adder is designed for low power and high performance. Different techniques like dual mode logic (DML) and dual mode addition (DMADD) are reported in open literature to consume low power and high speed. In this paper dual mode square adder which is a combination of DML and DMADD is implemented using static energy recovery full (SERF) adder. The performance of adder circuitsare compared with ripple carry adder using NAND gates. The Power dissipation of RCA using SERF adder is reduced by 42.62% compared to RCA using NAND gates and speed is increased by 82.3% using SERF Adder in dual mode square adder to RCA using NAND gates. Adders are implemented in mentor graphics tools in 130 nm technology.***

Index Terms: DML, DMADD, SERF Adder, Ripple carry adder, dual mode square adder.

I. INTRODUCTION

Addition is a basic operation in performing subtraction, division and multiplication. A adder using dual mode logic and dual mode addition is reported [1, 2],clock gating technique is used to optimize power in vlsi circuits by J. Shinde [3], the 64 bit adders implemented with CMOS compound domino logic, static CMOS and dynamic CMOS logic to obtain energy efficient design using circuit sizing and circuit design techniques [4-5], the n bit parallel adders are performed on a chip with regular layout by R. Brent and H. kung [6], a 32 bit carry look ahead adder is implemented using dual mode logic to achieve high speed [7], to achieve high speed low power high accurate (HP-LP-HA) adder is proposed by M.Parvathi [8], carry lookahead adder, carry skip adder and ripple carry adders are implemented using MT-CMOS technique to consume low power [9], the hybrid one bit full adder is designed using CMOS logic and transmission gate logic and the performance is analysed [10], in place of using regular two ripple carry adders, parallel prefix adder is used to design carry skip adder by PallaviSaxena [11].

In this paper low power and high performance DM^2 adder using SERF adder is implemented. DM^2 adder is a combination of DML and DMADD. The adder circuits are implemented using mentor graphics tools in 130 nm technology.

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II. ADDERS

Full adder: Full adder is a basic building block of the digital circuits. The inputs of full adder are A, B, and Ci and outputs are sum(S) and Carryout (Cout). The full adder can also be implemented by cascading of two half adders with an OR gate. The full adder using NAND gates is implemented as shown in Fig.1.

Sum = A xor B xorCi.

Carryout = (A xor B).Ci +A.B

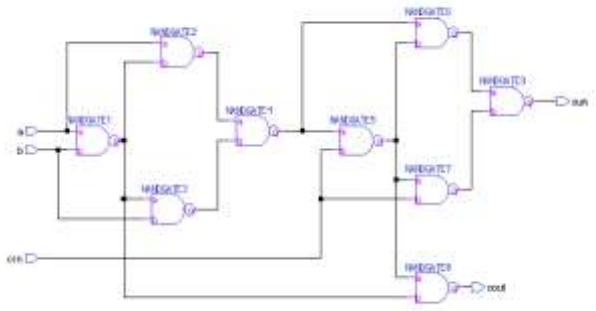


Fig.1Full adder Schematic diagram using NAND gates

SERF ADDER (Static Energy Recovery Full Adder): This is a modified full adder using ten transistors which achieves, low power dissipation and less delay when compared to the conventional designs. The modified full adder does not requires inverted inputs. This design is inspired by XNOR gates full adder design. The SERF adder has no direct path to ground, elimination of ground reduces the power dissipation. The implementation of SERF adder (schematic, simulated waveforms and layout) are shown in Figs. 2 to 4.

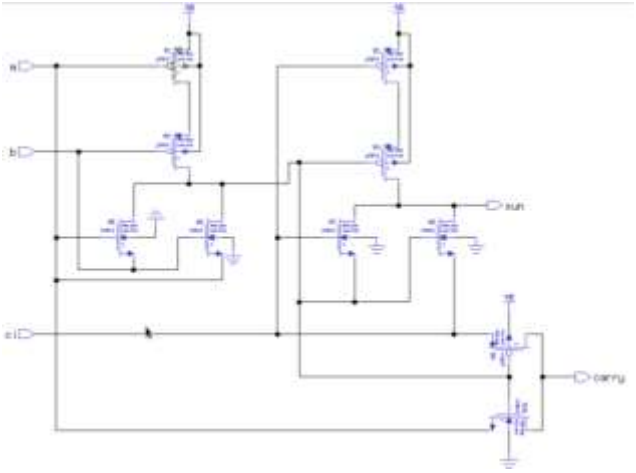


Fig.2 SERF Adder Schematic Diagram.

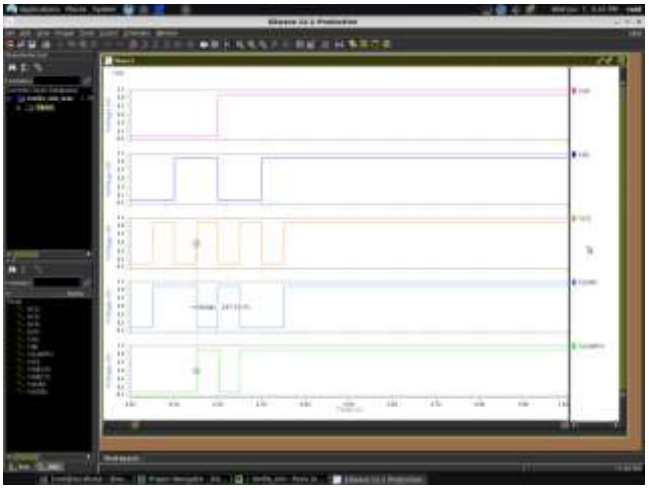


Fig.3 SERF Adder Simulated Waveforms

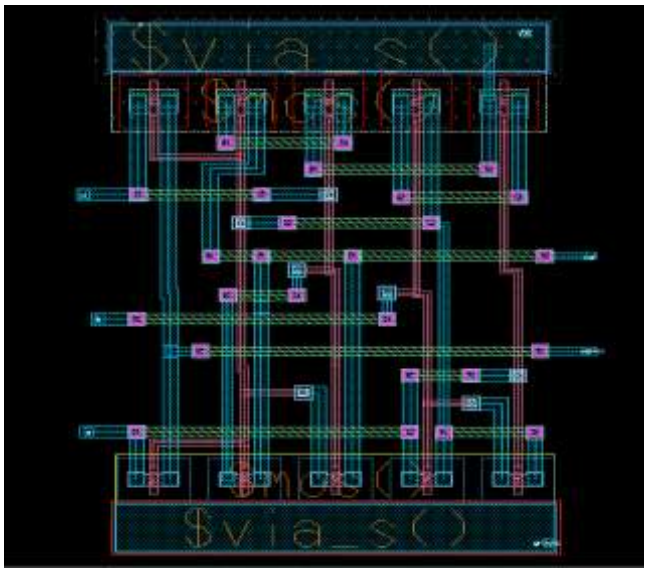


Fig.4 SERF adder layout

In view of the importance of low power dissipation and high speed two new techniques dual mode logic (DML) and dual mode addition (DMADD) to achieve low power and high speed are presented below.

Table.1 Comparison of 1bit full adder performance

Parameters	1 bit full adder using NAND gates	1 bit SERF adder
Power dissipation (watts)	50n	6n
Delay (sec)	291.25n	116.1p

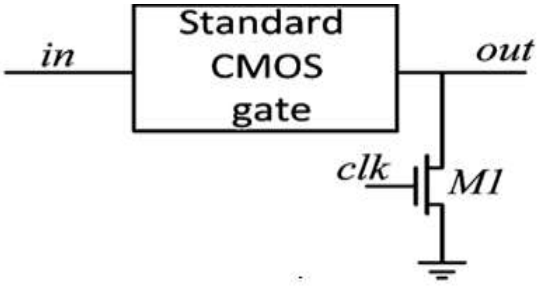
The comparison of 1 bit full adder performance is presented in Table 1. The one bit SERF adder achieves high speed (low delay) and low power dissipation compared to adder with NAND gates.

III. DUAL MODE LOGIC

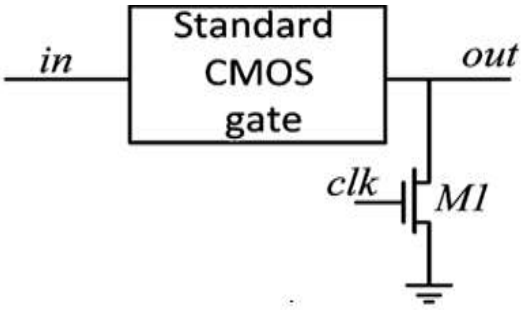
Dual Mode Logic gate is similar to static CMOS gate and an additional transistor. DML gate is simple and sizing scheme of transistor is required to achieve desired performance. In static mode it consumes less power and works faster in dynamic mode. Proper transistor sizing to achieve less power dissipation and less delay. Dual mode logic switches between operating modes i.e., static operating mode and dynamic operating mode. The gate of the additional transistor is connected to clock signal. The DML technique has four different topologies i.e., Type A, Type B, Headed and Footed topologies. The DML topologies are presented in Fig.5(a-d).

In static mode the clock transistor is always off the output depends on the operation of standard CMOS gate. In dynamic mode the clock enables and works in two modes precharge and evaluation modes. In TypeA DML topology the PMOS transistor is connected at the output. When the clock input is low the PMOS transistor (M1) conducts and the output is precharged to VDD. When high clock signal is applied to the PMOS transistor is applied M1 is cutoff the output depends on logic of the CMOS gate.

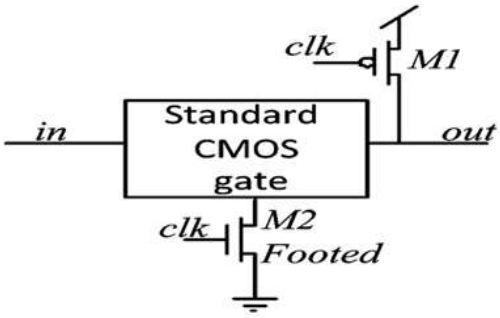
In TypeB DML topology the NMOS transistor is connected at the output with drain terminal to the ground. When the clock input is low the NMOS transistor M1is cutoff and the output depends upon the logic of standard CMOS gate. When the clock input is high the NMOS transistor conducts and the output is precharged to ground, thus the DML is operated in both static mode and dynamic modes. This dual mode logic achieves low power and high performance by working in static mode (low power) and dynamic mode (high performance).



a) Type A DML Topology



b) Type B DML Topology



c) Footed DML Topology

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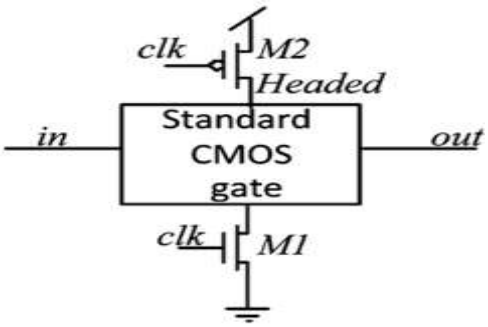

d) Headed DML topology

Fig.5 (a-d) DML Topologies

The SERF adder is implemented in four topologies of DML, schematics, simulated waveforms and layouts of all four topologies of DML using SERF adder are presented in Figs.6 to 13.

A. Implementation of Serf Adder using DML Topology:

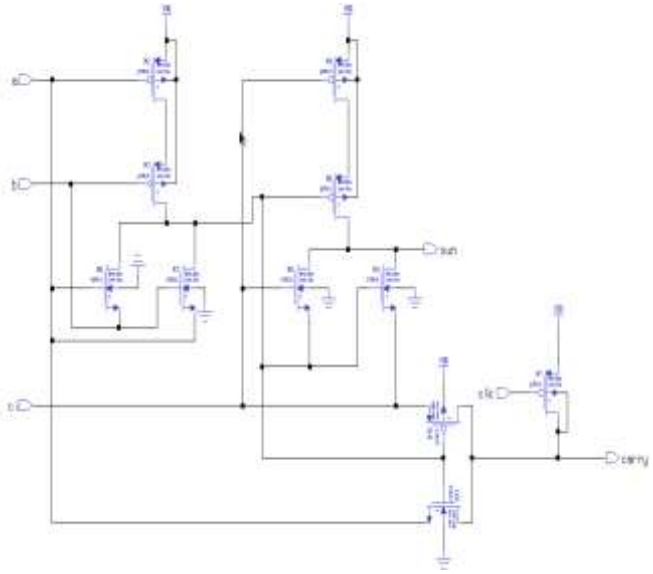

Fig.6 SERF adder schematic diagram using TypeA DML topology

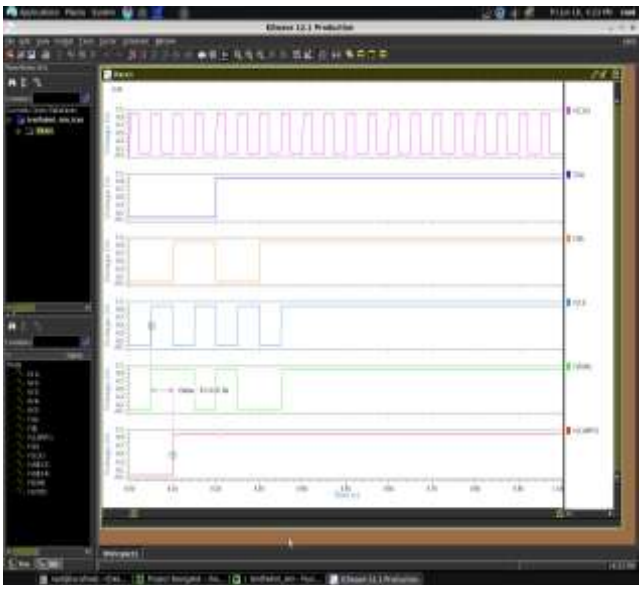

Fig.7 SERF adder simulation waveforms using TypeA DML topology

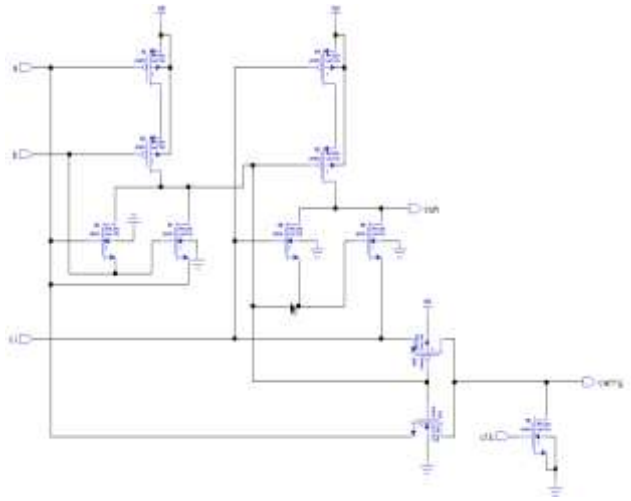

Fig.8 SERF adder schematic diagram using TypeB DML topology

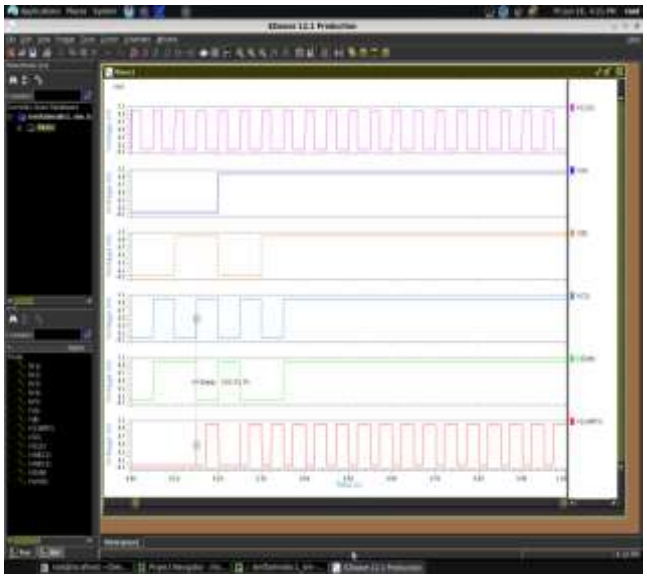

Fig.9 SERF adder simulation waveforms using TypeB DML topology

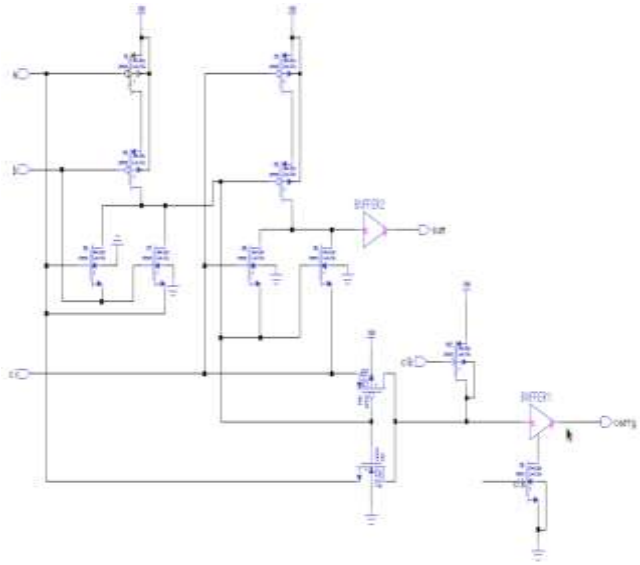

Fig.10SERF adder schematic diagram using footed DML topology

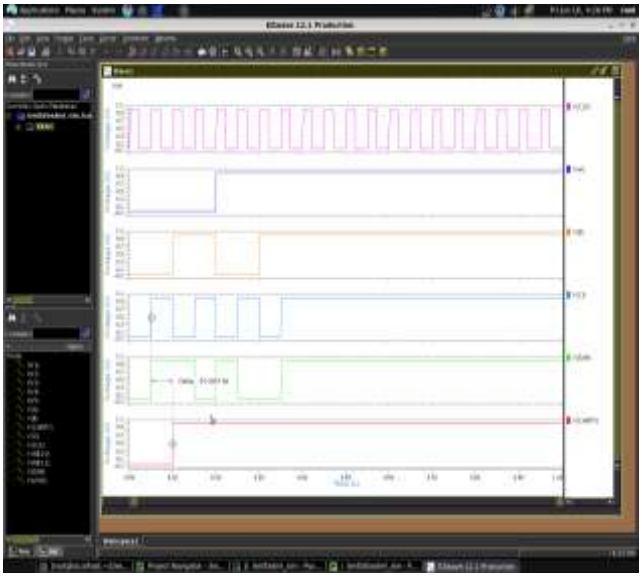

Fig.11 SERF adder simulation waveforms using footed DML topology

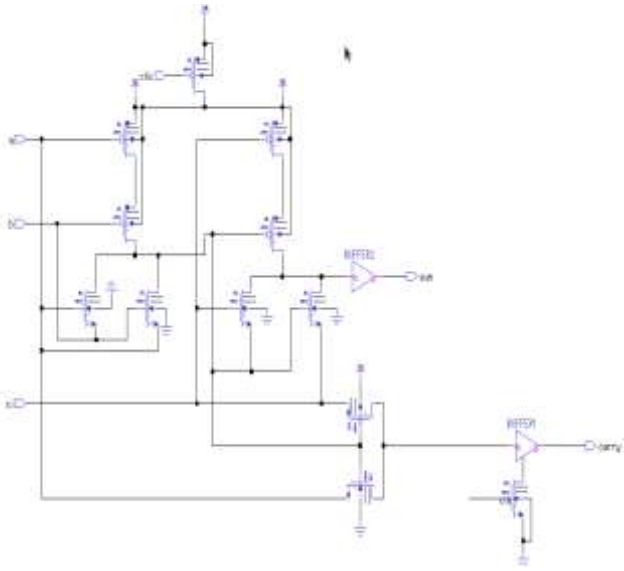

Fig.12 SERF adder schematic diagram using headed DML topology

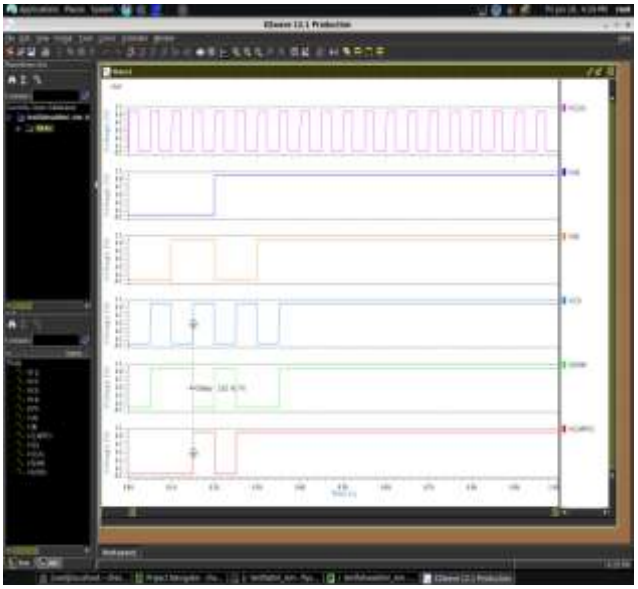

Fig.13 SERF adder simulation waveforms using footed DML topology

Table.2 Comparison of SERF adder using DML topology

Parameters	SERF ADDER				
	Conventional design	Type A DML	Type B DML	Headed DML	Footed DML
Power dissipation (watts)	6n	94u	3.2n	6.6n	96u
Delay (sec)	116.1p	49.54 n	49.52 n	49.54 n	49.54 n
Power delay product	6.972x 10^{-12}	4.656 x10^{-12}	1.58x 10^{-16}	3.269 x10^{-16}	4.755 x10^{-12}

Comparison of SERF adder performance in different DML topologies is presented in Table.2. TypeB DML topology consumes less power and achieves high speed, compared to other DML topologies.

*DUAL MODE ADDITION (DMADD)*achieves low power dissipation and works in two modes i) Normal addition mode ii) Extended addition mode. The DMADD topology is shown in Fig.14. The addition can be done using only one clock cycle by taking the advantage of carry probability which is called as Normal addition Mode. The second mode is extended mode which sometimes require more clock cycles to complete addition called as extended mode. Control circuit is required to decide whether to work in normal mode or in extended mode. This DMADD is used in pipelined processor. When DMADD is used in pipelined processor the control circuit is used to select the proper mode at instruction decode stage.

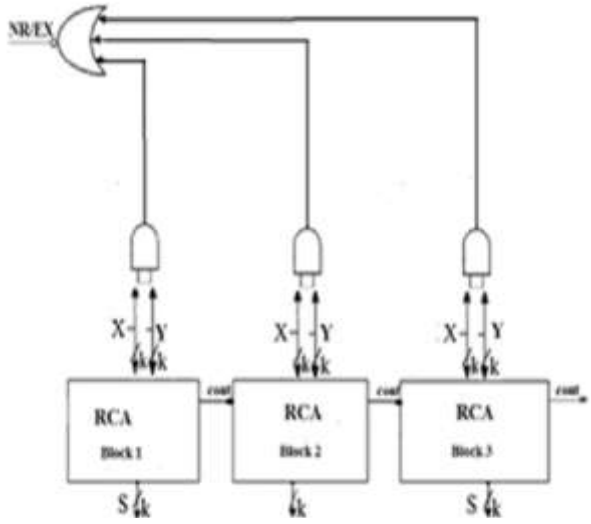

Fig.14 Dual Mode Addition Topology

The dual mode addition has design overhead and also consumes more power when compared to dual mode logic.

IV. DUAL MODE SQUARE ARCHITECTURE

The DM^2 square adder is combination of DML and DMADD. When DML logic is inserted in DMADD then it is called as dual mode square adder shown in Fig.15. Ripple Carry Adder is a main block in dual mode square adder.

For an n bit ripple carry adder the dual mode square adder is divided into m=n/k groups of k bits each. The carry does not propagate more than (2k-1) bits.

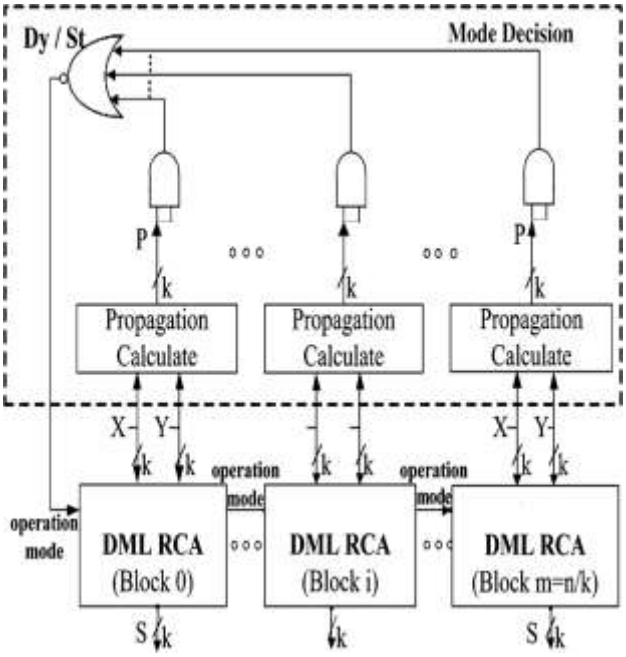

Fig.15Dual Mode Square Adder

The probability of carry is $m/2^k$ in extended mode through which it propagates 2k-1 bits. By doing the unconventional sizing of the transistor the carry path in worst case for n bit must completed in given clock cycle.

Ripple carry adder is a basic block in dual mode square adder. To overcome the disadvantage in dual mode addition and to consume low power, the dual mode logic and dual mode addition are combined to form dual mode square adder, using which high speed and low power dissipation can be achieved.

V. RIPPLE CARRY ADDER

Full adder is a basic unit of Ripple Carry adder. The Ripple Carry Adder can be extended to n number by connecting the carryout of previous full adder to the next full adder as input to Cin. An n-bit ripple carry adder consists of n number of single bit full adder. The delay depends on the carry propagation and it occupies less area and gives good performance. The full adders are cascaded in ripple carry adder by carry chain. The worst case delay of carry path is calculated from least significant bit (LSB) to most significant bit (MSB), and the delay increases linearly with increase in full adders. The implementation of ripple carry adder is shown in Figs.16 to 18.

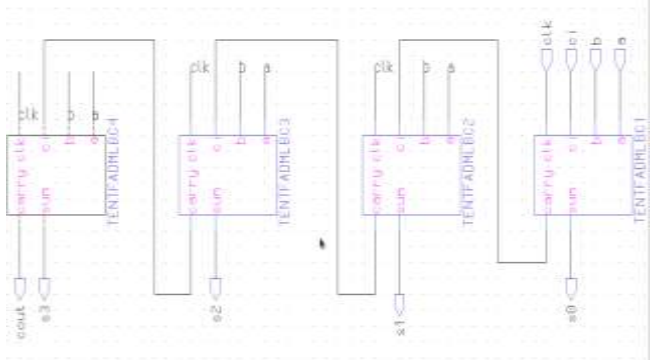

Fig.16 Ripple carry adder Schematic diagram

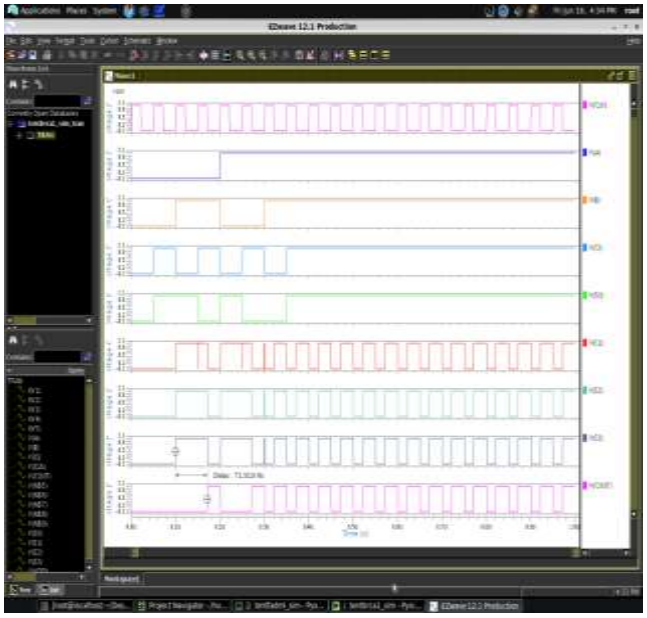

Fig.17Ripple carry adder simulation waveforms

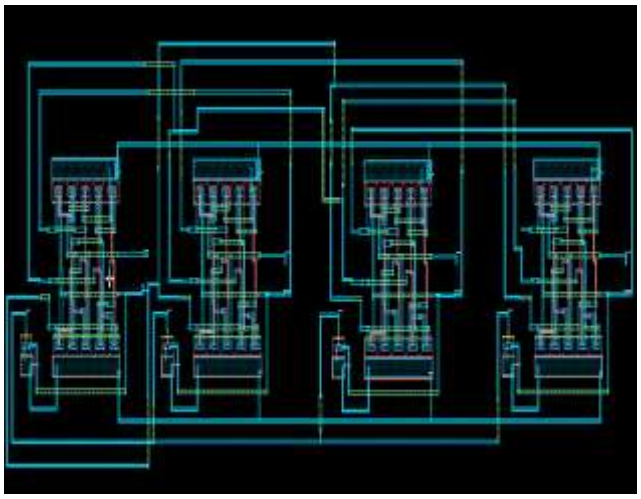

Fig.18Ripple carry adder layout

The dual mode square adder is implemented using SERF adder as basic full adder by inserting TypeB dual mode logic.

A. Dual mode square adder in TypeB DML topology:

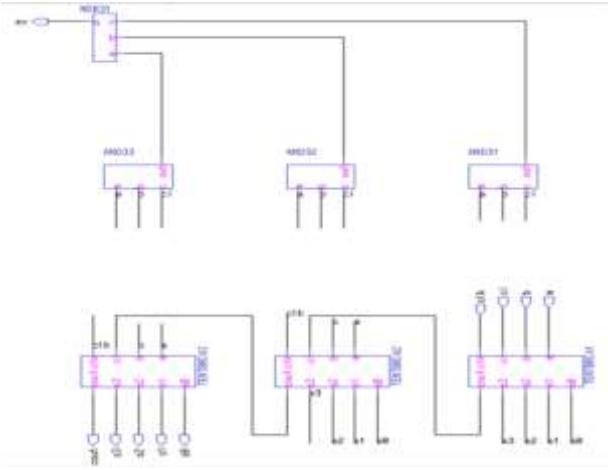

Fig.19 DM2 adder topology

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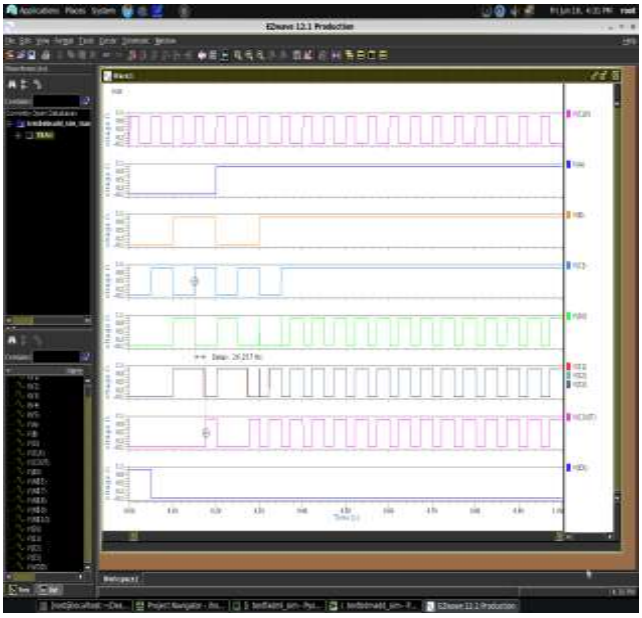

Fig.20 DM2 adder simulation waveforms

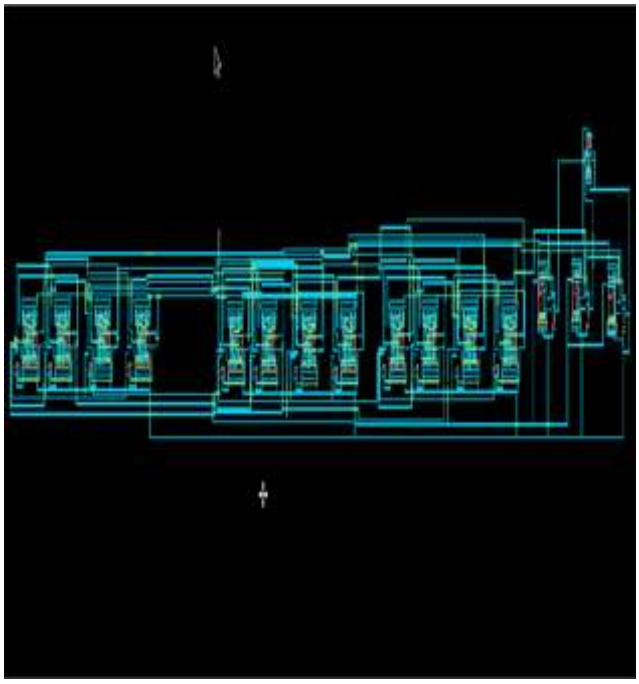

Fig.21 DM2 adder layout

Table.3 Comparison of the performance of different adders in different design topologies

Parameters	RCA using NAND gates	RCA using SERF adder	DM^2 adder
Power dissipation (watts)	24.4n	14n	57n
Delay (sec)	148n	50n	26.25n

Comparison of performance of adders in terms of power dissipation and delay are presented in Table 3.

From the results it is evident that the proposed RCA using SERF adder achieves less power dissipation and dual mode square adder using SERF adder with DML achieves high speed compared to RCA using NAND gates.

VI. CONCLUSION

Adders are implemented using different designs, ripple carry adder is implemented using SERF adder and dual mode square adder is implemented using RCA using SERF adder with DML topology. By comparing the RCA using SERF adder with RCA using NAND gates the power dissipation is reduced by 42.62%. For the dual mode square adder the speed is increased by 82% compared to RCA using NAND gates.

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