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Development of an Embedded System for Monitoring of Voltage and Current Harmonics

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Abstract*: Power quality has gained significant importance in the power industry over the past two decades. The increasing use of power electronic converters and various dynamic and nonlinear loads has adversely affected the quality of power, resulting in harmonic pollution. This pollution results in increased plant downtimes, reduced system efficiency, and elevated power losses. Harmonics refer to the frequency components of an electrical signal that are integer multiples of the fundamental frequency. In power systems, harmonic analysis is crucial for assessing the impact of harmonic-producing loads, and it plays a vital role in system planning, equipment design, and troubleshooting. Harmonics can cause detrimental effects such as conductor overheating, accelerated ageing of electrical insulation, and overall reduction in power efficiency. Among several techniques available for harmonic analysis, the Fast Fourier Transform (FFT) is the most used due to its computational efficiency. FFT is an algorithm that computes the Discrete Fourier Transform (DFT), which converts a finite set of discrete-time samples into their corresponding frequency-domain representation. This paper focuses on the voltage and current harmonics monitoring using a low-cost embedded processor. The proposed low-cost solution enables industries and utilities to implement harmonic monitoring systems cost-effectively, facilitating timely corrective actions to maintain power quality and system reliability.

Keywords: DFT, TMS320f28335 processor, Signal processing, Harmonics, Nonlinear load

Abbreviations:
FFT: Fast Fourier Transform
DFT: Discrete Fourier Transform
PLL: Phase-Locked Loop
THD: Total Harmonic Distortion
FPU: Floating-Point Unit
ADC: Analogue-to-Digital Converter
SCI: Serial Communication Interface
IDE: Integrated Development Environment
GUI: Graphical User Interface
RMS: Root Mean Square
ISR: Interrupt Service Routine

I. INTRODUCTION

The demand for electrical power is continuously rising with the increasing proliferation of electrical and electronic equipment in residential, commercial, and industrial sectors.

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To improve energy efficiency and control, power electronic converters are being extensively deployed in both home appliances and industrial applications. However, this widespread adoption of power electronics introduces significant distortion in the power system's voltage and current waveforms. The growing number of non-linear loads, high-speed switching devices, and other dynamic and distributed loads primarily causes the distortion.

In modern power systems, these dynamic loads have become more prevalent, resulting in higher harmonic content and greater complexity in power quality management. Harmonic analysis plays a crucial role in understanding the impact of such distortions and is extensively used in system planning, equipment design, and fault diagnosis.

To monitor harmonic levels in the system, specialized instruments such as power quality analyzers are typically employed. However, the high cost of these instruments often discourages utilities and industries from deploying them. As a result, many installations cannot continuously monitor harmonic levels, identify major harmonic components in voltage and current waveforms, and implement necessary mitigation strategies.

In addition to power electronic converters, various other electrical devices contribute significantly to harmonic distortion in power systems. Equipment such as appliances with magnetic cores, DC arc furnaces, fluorescent lamps, and LED lighting systems is known to be a source of harmonics. The presence of these harmonics can lead to several detrimental effects, including interference with communication, control, and protection systems, premature equipment ageing, and increased power losses throughout the system.

Among the available techniques for harmonic analysis, the Fast Fourier Transform (FFT) remains the most widely adopted due to its computational efficiency and ability to provide a comprehensive frequency-domain representation of electrical signals. FFT efficiently computes the Discrete Fourier Transform (DFT), allowing for the accurate determination of individual harmonic components.

Another method used for harmonic detection is the Phase-Locked Loop (PLL) technique [1]. While PLL-based detection can identify specific harmonic components, its primary limitation lies in its inability to detect multiple harmonic orders simultaneously. To analyze a range of harmonics—from the fundamental frequency up to the 25th harmonic (i.e., from 50 Hz to 1250 Hz in a 50 Hz system)—separate phase detectors must be implemented for each harmonic order. This not only increases system complexity but also necessitates precise tuning and calibration. Furthermore, the calculation of Total Harmonic Distortion (THD) requires additional logic when using PLL-based methods.

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The paper demonstrates the implementation of the FFT in digital signal processors, providing practical results.

II. HARMONICS CALCULATION USING THE FFT ALGORITHM

The computational problem for the DFT is to compute the sequence {X (k)} of N complex-valued numbers given another sequence of data {x(n)} of length N, according to (1)

$$X(k) = \sum_{n=0}^{N-1} x(n)\, W_N^{kn}, 0 \le k \le N-1 \quad \ldots \quad (1)$$

$$\text{Were, } W_N = e^{-j2\pi/N} \quad \ldots \quad (2)$$

To compute all N values of the DFT, N^2 complex multiplications and N^{2N} complex additions are required. Direct computation of the DFT is inefficient primarily because it does not exploit the symmetry and periodicity properties of the phase factor W_N. The two properties are

$$\text{Symmetry property: } W_N^{k+N/2} = -W_N^k \quad \ldots \quad (3)$$

$$\text{Periodicity property: } W_N^{k+N} = W_N^k \quad \ldots \quad (4)$$

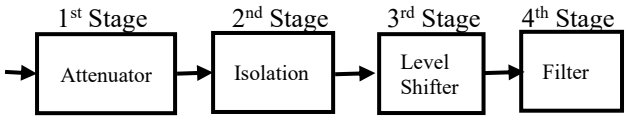
The FFT algorithm exploits these two basic properties of the phase factor. The computation of N-point DFT via the decimation-in-time FFT requires only (N/2) log 2N complex multiplications and Nlog2N complex additions. In this work, an 11-stage butterfly analysis is used to accommodate a total of 2048 samples from the ADC.

III. SIGNAL CONDITIONING

Signal conditioning is necessary to ensure that input signals are within the compatible range for the processor. The voltage sensing circuit is designed to handle up to 276 V RMS, while the current sensing circuit can measure up to 20 A RMS. The system operates at a frequency of 50 Hz.

A. Voltage Conditioning Circuit

The signal conditioning block comprises four stages that accurately sense and condition the input signals.



[Fig.1: Voltage Conditioning Circuit Block Diagram]

The system is designed to measure a nominal voltage of 230 V RMS, but to accommodate a possible 20% rise in grid voltage, it can measure up to 276 V RMS. The signal conditioning block comprises four stages:

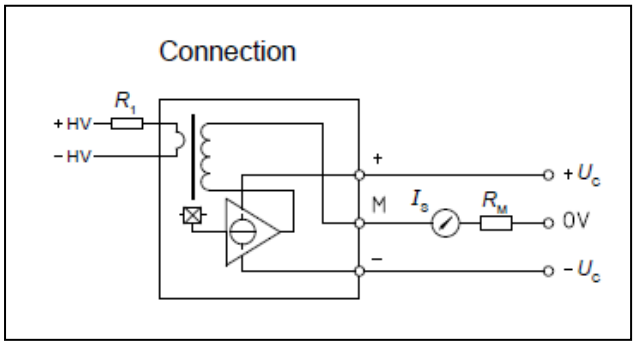
The first stage attenuates the input voltage to approximately 0.8 V RMS.

The second stage provides galvanic isolation between the high-voltage input and the low-voltage measurement circuitry.

Since the ADC can only sense positive voltages in the 0–3 V range, the third stage shifts the signal by 1.5 V and adjusts the gain accordingly.

The final stage filters out noise and delivers a clean, conditioned signal to the analogue-to-digital converter (ADC).

The above circuit utilises an LEM voltage sensor, specifically the LV25-P. The input resistance, R1, is set to 50 kω, allowing a 5-mA current to flow from the input and providing 0.8 V at the output.



[Fig.2: Wiring Connection for LEM Voltage Transducer]

A cost-effective method for voltage sensing is the use of a step-down transformer [2]. The transformer core must be carefully designed to ensure minimal no-load current draw. However, due to the core's nonlinearity, the signal may contain third-order harmonic distortion. Table I presents a comparison between the performance of a step-down transformer and an LEM sensor.

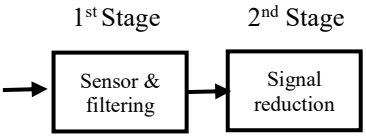
Table-I: Comparison Between Lem Sensor and the Step-Down Transformer

Sr. No.	Voltage Applied Through the Programmable Waveform Simulator	LEM Sensor Output	Step-Down Transformer Output
1	Voltage: 230 Vac	0.8 Vac	9.1 Vac
2	Voltage THD: 0.0 %	0.1 %	0.4 %
3	3rd order harmonics: 0.0 %	0.1 %	0.4 %

To eliminate third-order harmonic distortion caused by the step-down transformer, an LEM sensor is used for voltage sensing. Additionally, to protect the ADC from potential overvoltage due to an analogue system failure, a Zener diode is employed to clip the signal within safe limits.

B. Current Conditioning Circuit

The conditioning circuit for current sensing required two stages, as shown in Figure 3.



[Fig.3: Current Conditioning Circuit Block Diagram]

The first stage senses the current signal using a Hall Effect current transducer, model HXP 20-NP/SP30. This sensor outputs a signal centred at 2.5 V DC when the input current is zero. As current flows through the primary, the output voltage increases above 2.5 V. Since the processor's ADC operates within a 0–3 V range, the signal must be rescaled accordingly. A voltage divider, combined with an op-amp, is used to attenuate the signal, shifting the zero-current output level to 1.5 V DC.

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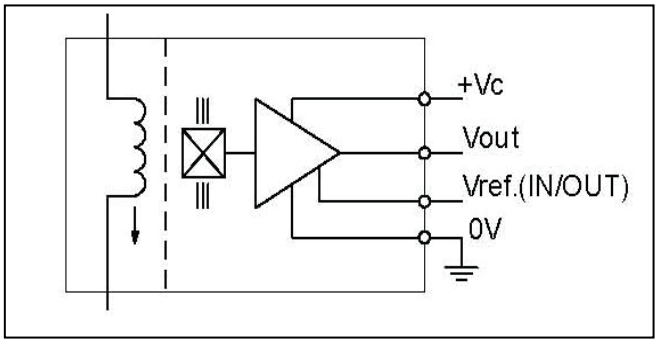


[Fig.4: Wiring Connection for LEM Current Transducer]

An anti-aliasing filter is implemented using an external 4.7 nF capacitor connected between the output (Vout) and ground. Like the voltage conditioning circuit, a 3.1 V Zener diode is placed at the output to protect the ADC from overvoltage conditions.

IV. PROCESSOR AND FFT IMPLEMENTATION

The processor used in this design is the TMS320F28335, a 32-bit microcontroller unit (MCU) with an integrated floating-point unit (FPU). The FPU enables higher precision in numerical computations and facilitates real-time signal analysis. The DSP operates at a clock frequency of 150 MHz. It features a 12-bit Analogue-to-Digital Converter (ADC) with a working range of 0–3 V and provides a total of 16 ADC channels [3].

Figure 5 presents the flowchart of the main program algorithm, which details the process of computing the Fast Fourier Transform (FFT) using 12-bit real-time ADC inputs to extract spectrum magnitude and phase information. The input data is acquired through an interrupt service routine. Conditioned voltage and current signals are fed into ADC channels 0 and 1, respectively—channel 0 is used for voltage harmonic analysis, and channel 1 for current harmonics. Sampling is triggered using the DSP's Enhanced Pulse-Width Modulation (ePWM) module to ensure precise timing for harmonic analysis. Upon system startup, all relevant DSP modules—including ePWM, GPIO, ADC clock, ADC registers, and ADC interrupts—are initialized.

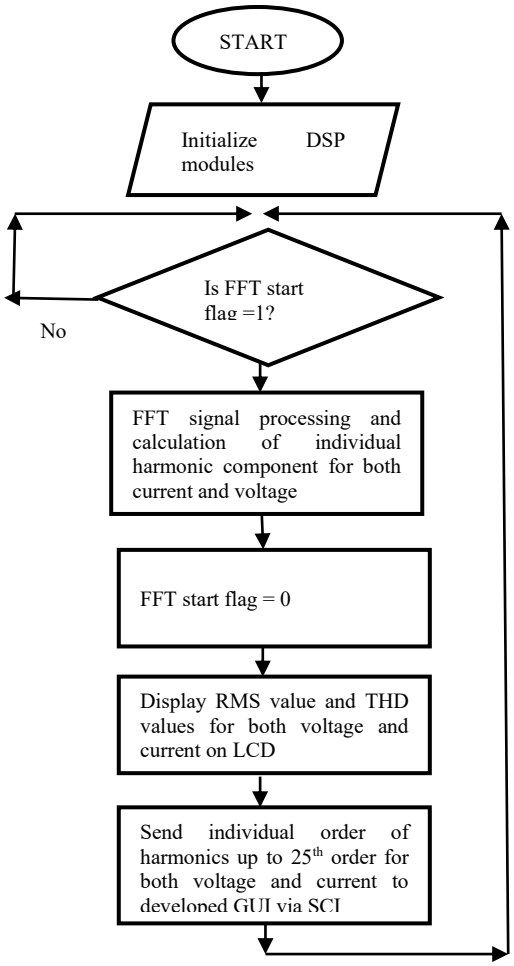
Once the FFT start flag is set to 1, FFT processing is initiated. The system can extract and store individual harmonics up to the 25th order in memory. After completing the calculations, the FFT start flag is reset to 0, allowing the next data frame to be processed. The buffered data is then displayed on a 20x4 LCD, showing RMS voltage, RMS current, and Total Harmonic Distortion (THD) for both voltage and current. Additionally, the individual harmonics up to the 25th order are transmitted to the developed Graphical User Interface (GUI) via the Serial Communication Interface (SCI).

The voltage THD and current THD are calculated according to (5) and (6), respectively.

$$V_{THD} = \sqrt{\frac{V_2^2+V_3^2+V_4^2+V_5^2+V_6^2+\dots}{V_1^2}} \quad \dots \quad (5)$$

$$I_{THD} = \sqrt{\frac{I_2^2+I_3^2+I_4^2+I_5^2+I_6^2+\dots}{I_1^2}} \quad \dots \quad (6)$$

The RMS values of voltage and current are calculated based on the THD values and individual harmonic orders.



[Fig.5: Flow Chart of the Main Program]

The flowchart in Figure 6 illustrates the ADC interrupt service routine (ISR). When the ADC interrupt is triggered, the samples are collected and stored in the ADC buffer. Once the required number of samples is gathered, the FFT start flag is set to 1. The ISR then returns control to the main program.

V. GRAPHICAL USER DEVELOPMENT

Four parameters are displayed on a 20x4 LCD: the RMS value of voltage, the RMS value of current, the THD of voltage, and the THD of current, as shown in Figure 7 [4].

To optimize processor usage, the Serial Communication Interface (SCI) module of the DSP is employed to transmit data over longer distances. The individual harmonic orders are transmitted via SCI and displayed as a percentage of the fundamental component on a GUI platform.

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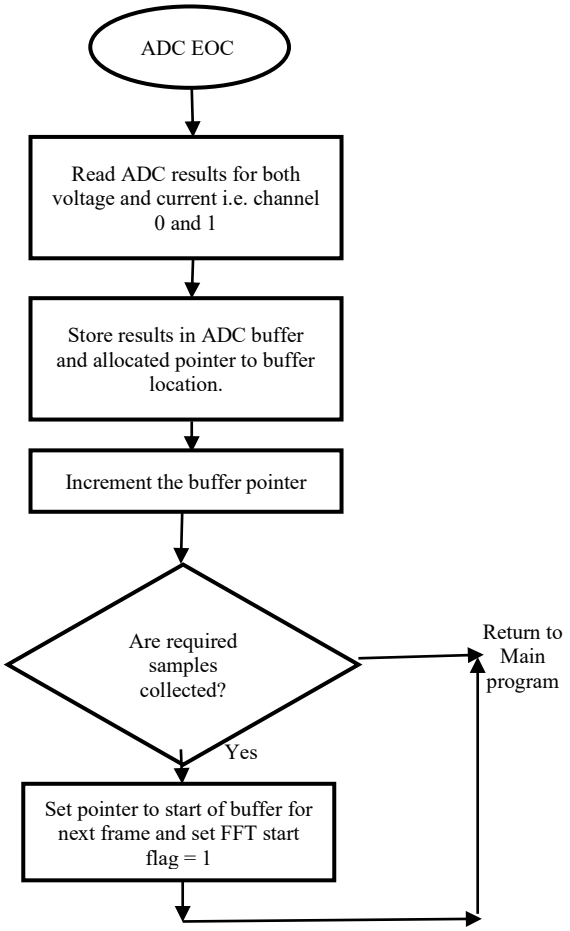
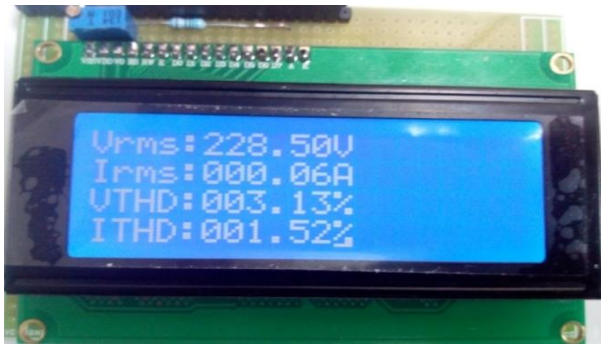
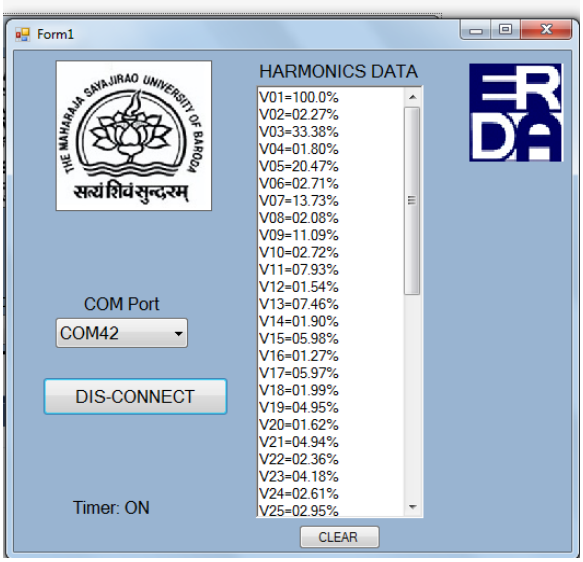


[Fig.6: Flow Chart of the ADC Interrupt Service Routine (ISR)]



[Fig.7: Display of Parameters on a 20 x 4 LCD]

The Graphical User Interface (GUI) was developed using Microsoft Visual Studio 2013, an integrated development environment (IDE) widely used for creating computer programs, websites, web applications, and mobile applications. Visual Studio offers a user-friendly platform for designing a graphical user interface (GUI) that receives and displays serial data. The baud rate is set to 19200 to ensure fast communication without data loss. The DSP transmits voltage and current harmonics up to the 25th order to the computer. The GUI allows the user to select the COM port for establishing communication between the DSP and the computer. Once the COM port is selected, the user must turn on the analyzer, which then begins displaying the harmonic orders. Figure 8 shows the display of harmonic orders in running mode.



[Fig.8: Running Mode of the GUI]

VI. EXPERIMENTAL SET UP

The validation of the developed hardware and software system is carried out through three experiments to assess its performance:

A. Validation using a programmable waveform simulator.
B. Measurement of no-load current harmonics in the transformer as per IS 2026 Part I: 2011 [5].
C. Measurement of output voltage harmonics from the inverter."

A. Validation Through Programmable Waveform Simulator

A programmable waveform simulator is used to generate the root mean square (RMS) values of voltage, current, and total harmonic distortion (THD). Tables II and III present the validation results for voltage and current, respectively. The programmable waveform simulator is calibrated with an accuracy of 0.05%, while the power meter used for comparison has an accuracy of 0.1%. The results are compared based on the test setup shown in Figure 9.

Table-II: Validation of the Developed Embedded System for a Voltage Signal

Voltage: 230 Vrms, 50 Hz			
Parameters	**Programmable waveform simulator**	**Power meter display**	**Developed an embedded system display**
Voltage	230.000 V	230.01 V	230.06 V
THD	46.15 %	46.18 %	46.04 %
Voltage: 250 Vrms, 50 Hz			
Parameters	**Programmable waveform simulator**	**Power meter display**	**Developed an embedded system display**
Voltage	250.000 V	250.12 V	250.09 V
THD	12.11 %	12.13 %	12.25 %

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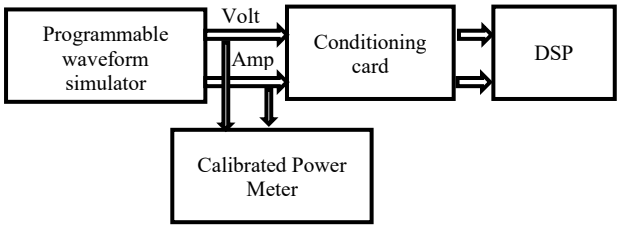
Table-III: Validation of the Developed Embedded System for the Current Signal

Current: 5 Arms, 50 Hz			
Parameters	**Programmable Waveform Simulator**	**Power Meter Display**	**Developed an Embedded System Display**
Current	5.000 A	5.01 A	5.10 A
THD	46.15 %	46.15 %	46. 24 %
Current: 10 Arms, 50 Hz			
Parameters	**Programmable Waveform Simulator**	**Power Meter Display**	**Developed an Embedded System Display**
Current	10.000 A	10.02 A	10.15 A
THD	12.11 %	12.15 %	12.21 %

The results show that readings displayed by the calibrated power meter and the developed embedded system are closely matching.

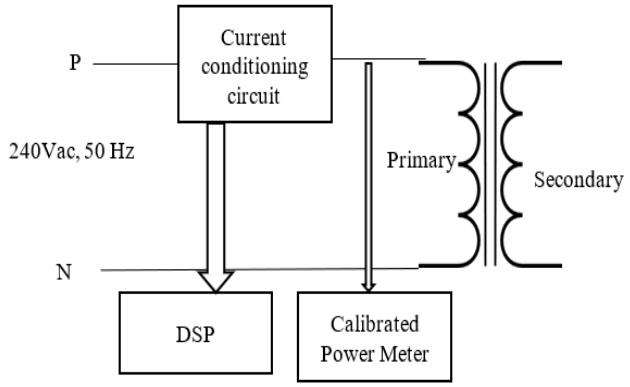


[Fig.9: Test set up Diagram]

B. Measurement of no-load Current Harmonics of the Transformer as per IS 2026 Part I: 2011

Clause 10.6 of IS 2026 Part I: 2011 defines the procedure for measuring no-load current harmonics. The objective of this test is to assess the harmonics generated by the core material used in the transformer.

For this test, a 5 kVA transformer is used. One winding, either the primary or secondary, is left open-circuited, and the rated voltage is applied to the transformer. The no-load current drawn by the transformer injects harmonics, with the dominant harmonic orders being the 3rd and 5th, corresponding to 150 Hz and 250 Hz, respectively. The test setup is shown in Figure 10.



[Fig.10: Test Set up Diagram]

Table IV presents the results of the harmonics obtained through the test, compared with those of a calibrated power meter.

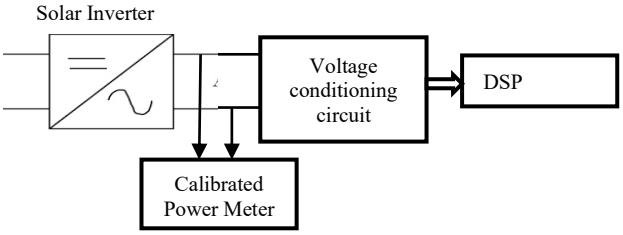
Table-IV: Comparison of Harmonics with the Power Meter and the Designed System

Harmonic Order	Calibrated Power Meter Readings		Developed Embedded System Readings	
	Current in %.	*Voltage in %*	*Current in %.*	*Voltage in %*
1	100.00	100.00	100.00	100.00
2	0.80	0.05	0.78	0.05
3	58.45	0.87	58.25	0.87
4	0.31	0.01	0.30	0.02
5	25.04	0.40	25.21	0.40
6	0.15	0.02	0.15	0.02
7	5.87	0.29	5.82	0.29
8	0.26	0.01	0.21	0.01
9	1.27	0.57	1.29	0.57
10	0.14	0.01	0.14	0.01
11	1.83	0.44	1.81	0.44
THD %	63.90	1.23	63.76	1.25
Parameter measured	191.37 mA	240.47 V	191.24 mA	240.41 V

The results from the calibrated power meter and the developed embedded system are found to match closely.

C. Measurement of Voltage Harmonics of 25 kVA Inverter

Switching components such as thyristors and diodes in inverters can inject harmonics into the system. To evaluate the performance of the developed embedded system, the output voltage harmonics of the inverter are measured and compared with a calibrated power meter. In this case, only the voltage harmonics are sensed and compared. The setup for the measurement is shown in Figure 11.



[Fig.11 Test Set up Diagram]

Table V presents the measurement results. The results are within the limits specified in IEEE 519:2014 [6].

Table-V: Measurement Result for Inverter Output Harmonics

Parameters	Power Meter Display	Developed an Embedded System Display
Voltage	229.12 V	228.50 V
THD	3.06 %	3.13 %

The results indicate that the developed embedded system yields readings comparable to those of a calibrated power meter.

VII. CONCLUSION

This paper presents the implementation of the FFT algorithm using the TMS320F28335 DSP. It also discusses the requirements for the signal conditioning circuit and its design for interfacing with the digital signal processor (DSP). Additionally, the paper describes the GUI developed in Microsoft Visual Studio, including it's communication with the DSP. Individual harmonic orders are transmitted to the

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computer via SCI and displayed on the GUI.

The validation of the developed embedded system was conducted through three different experiments. In all cases, the results from the embedded system closely matched those of a calibrated power meter. The developed embedded system is cost-effective and offers significant potential for real-time harmonic monitoring in various systems.

DECLARATION STATEMENT

After aggregating input from all authors, I must verify the accuracy of the following information as the article's author.

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- **Ethical Approval and Consent to Participate:** The content of this article does not necessitate ethical approval or consent to participate with supporting documentation.
- **Data Access Statement and Material Availability:** The adequate resources of this article are publicly accessible.
- **Author's Contributions:** The authorship of this article is contributed equally to all participating individuals.

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Bhavna Pancholi, having a PhD in Electrical Engineering, an M.E. in Electrical Engineering, and a B.E. in Electronics, has published 25 journal papers and seven conference papers. She has been in the teaching field for the last 25 years and has taught various electronics subjects. She wrote papers in the field of VLSI and face detection methods. She is working as an Assistant Professor at the Maharaja Sayajirao University of Baroda, Gujarat. She has expertise in the field of digital signal processing, particularly with TMS320F28335 DSP processors. She has done programming in embedded C and Python for various DSP projects. She has guided more than 20 students for the M.E. projects.

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